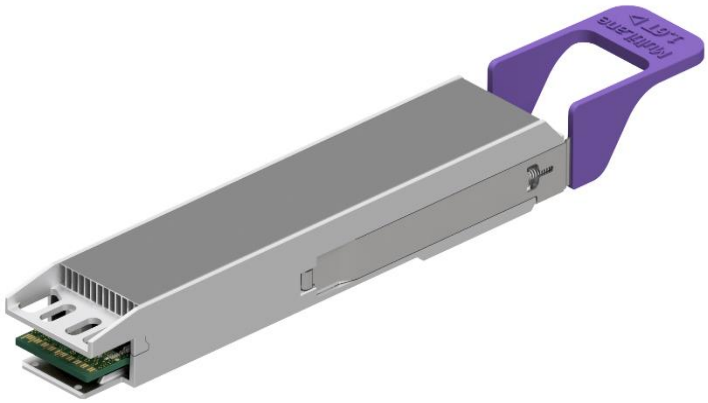
ML4064-AL7I/R-224

RevB

Technical Reference

OSFP Electrical Active Loopback Module

CMIS 5.2 Compliant



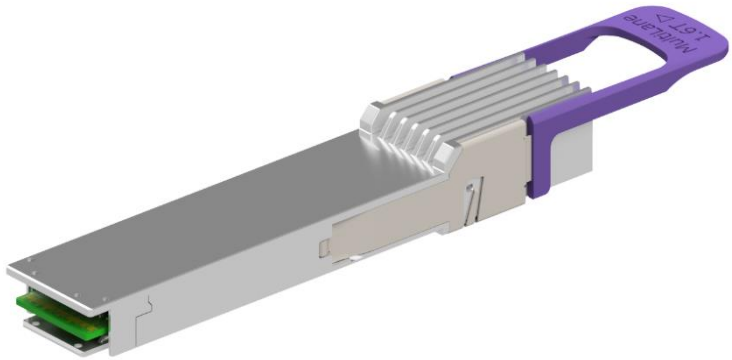


Table of Contents

1 Overview

The **ML4064-AL7I/R-224** is an OSFP active electrical loopback module that provides a straightforward method to test OSFP ports at every level of the switch production process. The active electrical loopback (ALB) includes a transceiver chip, where 8xTX channels and 8xRX channels are available. Data is transmitted from the host to the TX input port of the active loopback, and the retimed signal is received by the host via the RX output port of the active loopback. The **ML4064-AL7I/R-224** is ideal for R&D validation, production testing, and field testing. The **ML4064-AL7I/R-224** follows the **CMIS Rev 5.2** standard and is packaged in standard MSA housing compatible with all OSFP power classes.

1.1 ML4064-AL7I/R-224 OSFP active loopback | Key Features

- OSFP MSA Form Factor
- CMIS Compatible Configuration and EEPROM
- Programmable CMIS memory pages
- Custom memory maps
- I2C Interface
- Electrical transceiver chip
- Two temperature sensors
- Voltage sensor
- Cut-off temperature preventing module overheating
- Programmable power dissipation
- True insertion counter
- Firmware upgrade capability through CDB

LED Indicator

Green (Solid) – Signifies that the module is operating in high power mode.
Red (Solid) – Signifies the module is operating in low power mode.
Green (Blinking) – Signifies the module Temperature or Voltage alarm and warning is triggered, and module is operating in high power mode.
Red (Blinking) – Signifies the module Temperature or Voltage alarm and warning is triggered, and module is operating in low power mode.

1.2 Recommended Operating Conditions

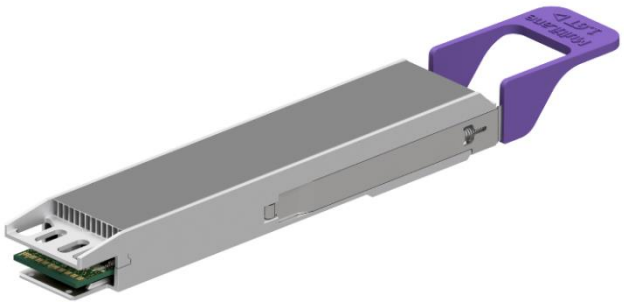
Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature (*)	T		0		100	°C
Supply Voltage	VCC	Main Supply Voltage	3.15	3.3	3.55	V
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω

(*) based on module internal temperature

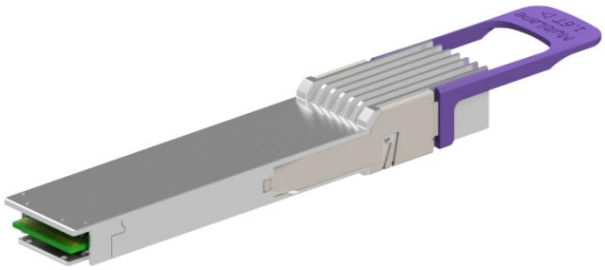
2 Ordering Options

The ordering options of the ML4064-AL7I/R-224 is detailed in the table below:

Option	Part Number	Description
IHS	ML4064-AL7I-224	OSFP IHS shell option
RHS	ML4064-AL7R-224	OSFP RHS shell option



ML4064-AL7I-224



ML4064-AL7R-224

3 Management Data Interface – I2C

The **ML4064-AL7I/R-224** supports the I2C interface.

3.1 I2C Signals, Addressing and Frame Structure

3.1.1 I2C Frame

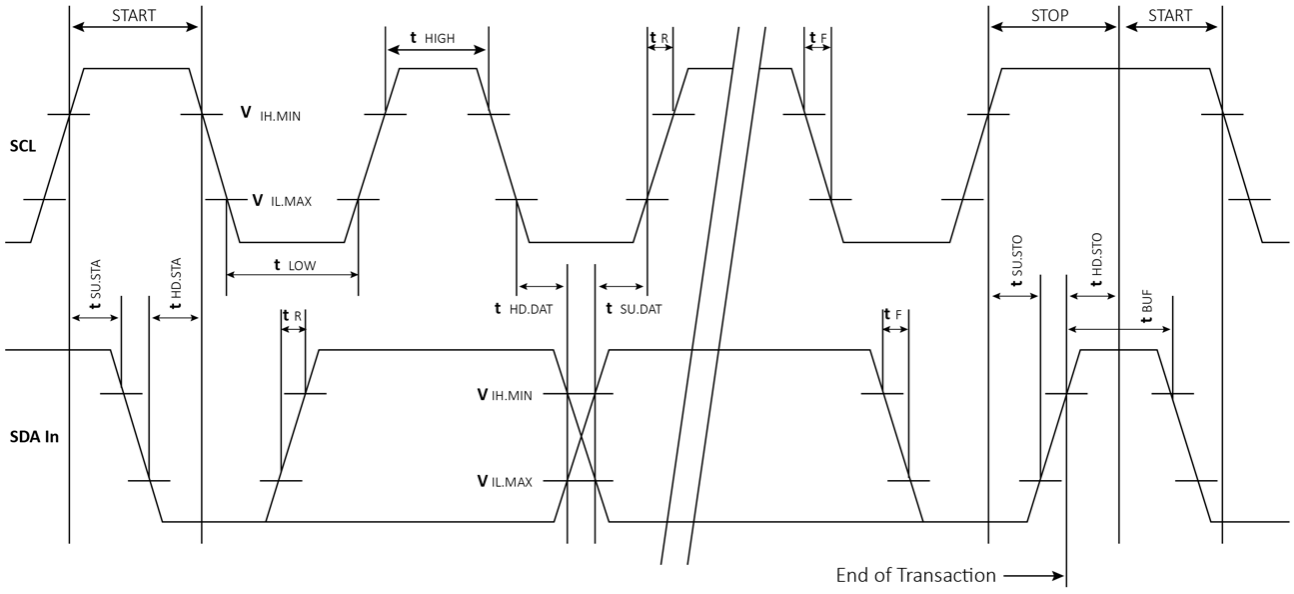


Figure 1: OSFP Timing Diagram

Parameter	Symbol	Min	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		125	us
Complete Single Write	tWR		40	ms

3.1.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the OSFP module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	10	1015	kHz
Clock Pulse Width Low	t_{LOW}	0.35		us
Clock Pulse Width High	t_{High}	0.35		us
Time Bus Free Before New Transmission Can Start	t_{BUF}	1.5		us
START Hold Time	$t_{HD.STA}$	0.08		us
START Set-up Time	$t_{SU.STA}$	0.4		us
Data In Hold Time	$t_{HD.DAT}$	0.1		us
Data In Set-up Time	$t_{SU.DAT}$	0.1		us
STOP Set-up Time	$t_{SU.STO}$	0.4		us

Maximum time the OSFP Module may hold the SCL line low before continuing with a read or write operation is 500us.

3.1.3 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to OSFP transceivers is used to positive-edge clock data into each OSFP device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven.

Master/Slave: OSFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each OSFP is hard wired at the device address A0h.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicating a START or STOP condition. All addresses and data words are serially transmitted to and from the OSFP in 8-bit words. Every byte on the SDA line must be 8-bit long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host are acknowledged by OSFP transceivers. Read data bytes transmitted by OSFP transceivers should be acknowledged by the host for all but the final byte read, for which the host should respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the OSFP management interface can be reset. Memory reset is intended only to reset the OSFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: OSFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 1. This is common to all OSFP devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: OSFP Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the OSFP transceiver output a zero (ACK) on the SDA line to acknowledge the address.

3.2 OSFP Memory Map

3.2.1 Full Map

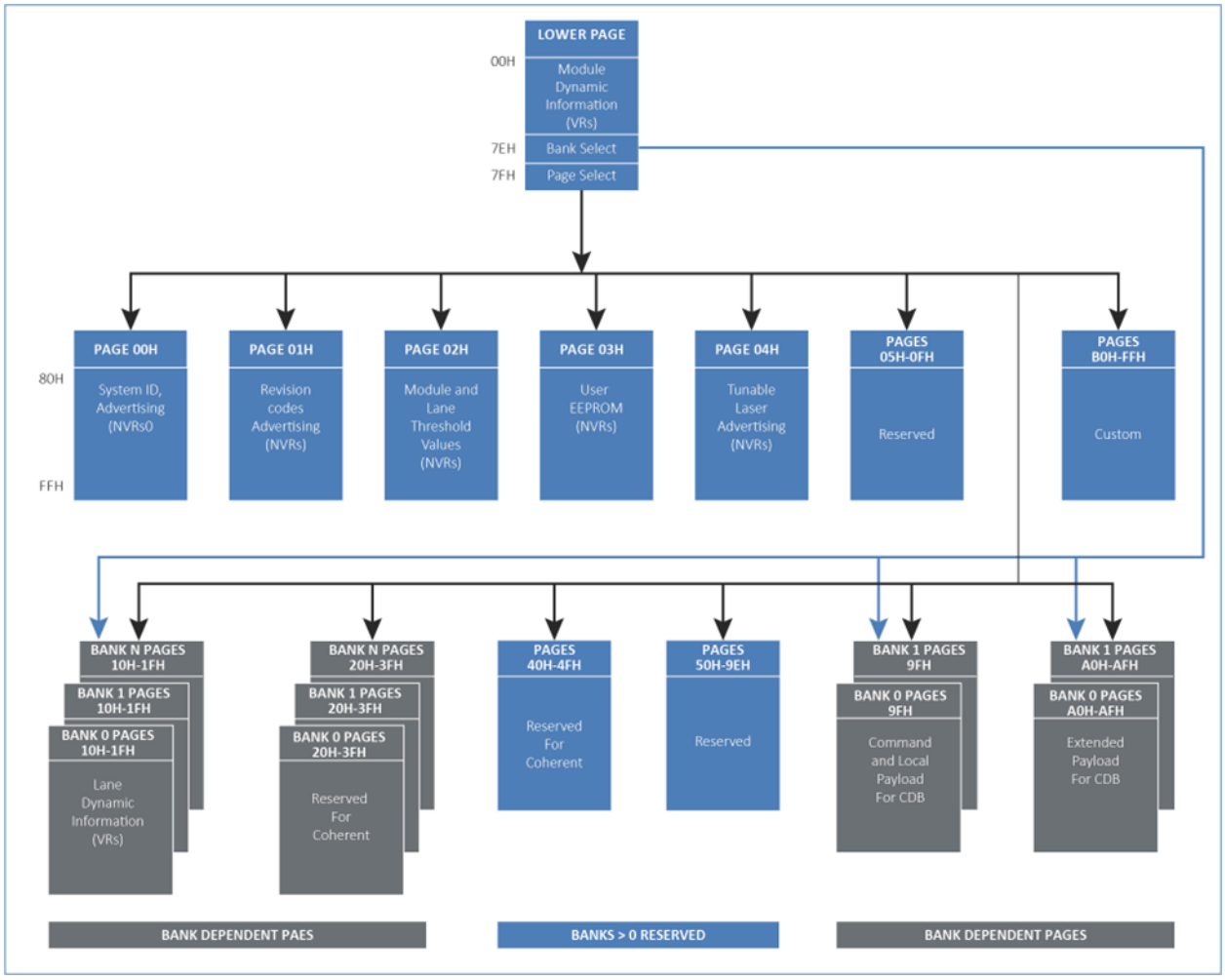


Figure 3: OSFP Memory Map

This section defines the Memory Map for OSFP transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all OSFP devices.
The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

3.2.2 ML4064-AL7I/R-224 Memory Map

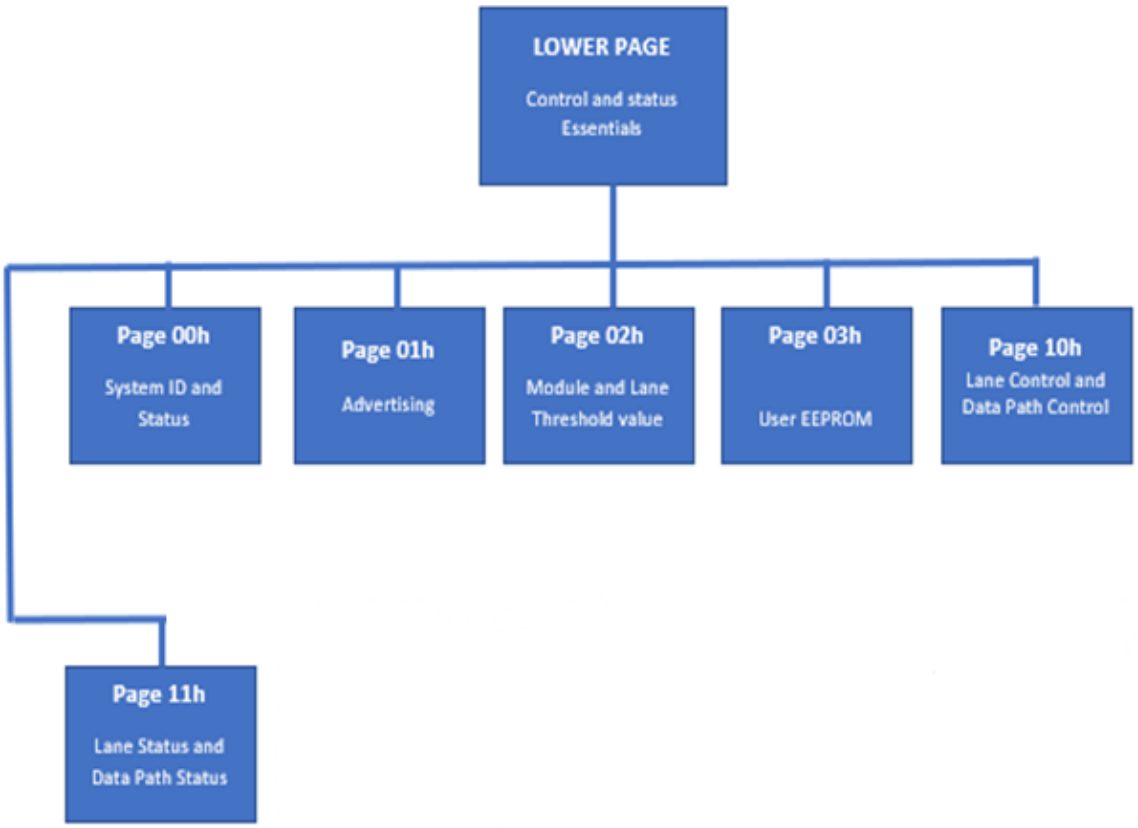


Figure 4: Implemented Memory Map

3.2.3 Memory Content

The table below shows the memory content.

Address	Hex	Decimal	ASCII	MSA Description
LowMem 0(00h)	0x19	25		Identifier
LowMem 1(01h)	0x52	82	R	Revision Compliance
LowMem 2(02h)	0x04	4		CLEI code present
LowMem 3(03h)	0x06	6		Module State
LowMem 4(04h)	0x00	0		Bank 0 flag summary
LowMem 5–7 (05h–07h)	0x00	0		Not Implemented
LowMem 8(08h)	0x00	0		Latched module state and FW error
LowMem 9(09h)	0x00	0		Latched VCC3.3/Temp Alarm and Warning
LowMem 10(0Ah)	0x00	0		Not implemented
LowMem 11(0Bh)	0x00	0		Latched Vendor Defined/AUX3 Alarm and Warning
LowMem 12(0Ch)	0x00	0		Reserved
LowMem 13(0Dh)	0x00	0		Custom
LowMem 14(0Eh)				Case Temperature MSB

LowMem 15(0Fh)				Case Temperature LSB
LowMem 16(10h)				Internally measured Supply 3.3v MSB
LowMem 17(11h)				Internally measured Supply 3.3v LSB
LowMem 18(12h)				Current consumption MSB
LowMem 19(13h)				Current consumption LSB
LowMem 20-23(14h-17h)	0x00	0		
LowMem 24(18h)				DSP Internally measured Temperature MSB
LowMem 25(19h)				DSP Internally measured Temperature LSB
LowMem 26(1Ah)	0x40	64		Software reset
LowMem 27-30 (1Bh-1Eh)	0x00	0		
LowMem 31-32 (1Ff-20f)	0x00	0		Masks for Alarms and warning
LowMem 39(27h)	0x01	1		Major FW Rev
LowMem 40(28h)	0x00	0		Minor FW Rev
LowMem 41-84 (29h-54h)	0x00	0		
LowMem 85(55h)	0x04	4		Media Type
LowMem 86(56h)	0x80	128		Host Interface ID AppSel code 1
LowMem 87(57h)	0xBF	191		Media Interface ID AppSel code 1
LowMem 88(58h)	0x11	17		Host and Media Lane Count AppSel code 1
LowMem 89(59h)	0xFF	255		Host Lane Assignment Options AppSel code 1
LowMem 90(5Ah)	0x81	129		Host Interface ID AppSel code 2
LowMem 91(5Bh)	0xBF	191		Media Interface ID AppSel code 2
LowMem 92(5Ch)	0x22	34		Host and Media Lane Count AppSel code 2
LowMem 93(5Dh)	0x55	85		Host Lane Assignment Options AppSel code 2
LowMem 94 (5Eh)	0x82	130		Host Interface ID AppSel code 3
LowMem 95 (5Fh)	0xBF	191		Media Interface ID AppSel code 3
LowMem 96 (60h)	0x44	68		Host and Media Lane Count AppSel code 3
LowMem 97 (61h)	0x11	17		Host Lane Assignment Options AppSel code 3
LowMem 98 (62h)	0x83	131		Host Interface ID AppSel code 4
LowMem 99 (63h)	0xBF	191		Media Interface ID AppSel code 4
LowMem 100 (64h)	0x88	136		Host and Media Lane Count AppSel code 4
LowMem 101 (65h)	0x01	1		Host Lane Assignment Options AppSel code 4
LowMem 102 (66h)	0x51	81		Host Interface ID AppSel code 5
LowMem 103 (67h)	0xBF	191		Media Interface ID AppSel code 5
LowMem 104 (68h)	0x88	136		Host and Media Lane Count AppSel code 5
LowMem 105 (69h)	0x01	1		Host Lane Assignment Options AppSel code 5
LowMem 106 (6Ah)	0x52	82		Host Interface ID AppSel code 6
LowMem 107 (6Bh)	0xBF	191		Media Interface ID AppSel code 6

LowMem 108 (6Ch)	0x88	136		Host and Media Lane Count AppSel code 6
LowMem 109 (6Dh)	0x01	1		Host Lane Assignment Options AppSel code 6
LowMem 110 (6Eh)	0x4F	79		Host Interface ID AppSel code 7
LowMem 111 (6Fh)	0xBF	191		Media Interface ID AppSel code 7
LowMem 112 (70h)	0x44	68		Host and Media Lane Count AppSel code 7
LowMem 113 (71h)	0x11	17		Host Lane Assignment Options AppSel code 7
LowMem 114 (72h)	0x50	80		Host Interface ID AppSel code 8
LowMem 115 (73h)	0xBF	191		Media Interface ID AppSel code 8
LowMem 116 (74h)	0x44	68		Host and Media Lane Count AppSel code 8
LowMem 117 (75h)	0x11	17		Host Lane Assignment Options AppSel code 8
LowMem 118–125 (76h–7Dh)	0x00	0		Password area
LowMem 126(7Eh)	0x00	0		Not Implemented
LowMem 127(7Fh)	0x00	0		Page Select Byte
Page00 128(80h)	0x19	25		Identifier
Page00 129–144 (81h–90h)		MULTILANE (ASCII)		Vendor Name
Page00 145–147 (91h–93h)	0x00	0		Vendor OUI
Page00 148–163 (94h–A3h)		ML4064-AL7I-224 (ASCII)		Vendor PN
Page00 164(A4h)	0x32	50	2	Vendor Rev
Page00 165(A5h)	0x30	48	0	Vendor Rev
Page00 166–181 (A6h–B5h)				Vendor SN
Page00 182–189 (B6h–BDh)		26030201 (ASCII)		Date Code
Page00 190–199 (BEh–C7h)	0x20	32		CLEI Code
Page00 200(C8h)	0xE0	224	`	Module Power Characteristics
Page00 201(C9h)	0xAC	172		Module Max Power Consumption
Page00 202–212 (CAh–D4h)	0x00	0		
Page00 213-220 (D5h-DCh)	0x00	0		Reserved
Page00 221(DDh)	0x00	0		Custom
Page00 222(DEh)				Checksum
Page00 223-255 (DFh-FFh)	0x00	0		Custom Info NV
Page01 128(80h)	0x00	0		Inactive Major FW Rev
Page01 129(81h)	0x00	0		Inactive Minor FW Rev
Page01 130(82h)	0x02	2		Module Major HW Rev
Page01 131(83h)	0x01	1		Module Minor HW Rev
Page01 132-141(84h-8Dh)	0x00	0		Not implemented
Page01 142(8Eh)	0x24	36		Supported Pages
Page01 143(8Fh)	0x7F	127	?	ModSelL setup time

Page01 144(90h)	0x77	119		Max Duration DPDeinit/DPInit
Page01 145(91h)	0x00	0		Module Characteristics advertising
Page01 146(92h)	0x55	85	U	Module TempMax
Page01 147(93h)	0x00	0		Module TempMin
Page01 148-149(94h-95h)	0x00	0		Not Implemented
Page01 150(96h)	0x91	145	?	OperatingVoltageMin
Page01 151(97h)	0x00	0		Not Implemented
Page01 152(98h)	0x00	0		CDRPowerSavedPerLane
Page01 153(99h)	0XF0	240		RxOutput Level Supported
Page01 154(9Ah)	0x77	119		RXOutput EQ Supported
Page01 155(9Bh)	0x01	1		Squelch method
Page01 156(9Ch)	0x03	3		Output Disable & PolarityFlipRx Supported
Page01 157(9Dh)	0x06	6		TX LOS Flag support
Page01 158(9Eh)	0x00	0		Not Implemented
Page01 159(9Fh)	0x23	35	#	Supported Monitors Advertisement
Page01 160(A0h)	0x00	0		Not Implemented
Page01 161(A1h)	0x08	8		TxInput Adaptive EqSupported
Page01 162(A2h)	0x1C	28		Rx Output Eq Control Supported
Page01 163 (A3h)	0x57	87		Cdb Instances Adv
Page01 164 (A4h)	0xFF	255		Cdb Read Write Length Extension
Page01 165 (A5h)	0x04	4		Cdb Command Trigger Method
Page01 166 (A6h)	0x80	128		Cdb Max Busy spec
Page01 167 (A7h)	0x77	119		MaxDurationModulePwrDn/Up
Page01 168-175(A8h-AFh)	0x00	0		MaxDurationnDPTxTurnOff/On
Page01 176(B0h)	0x01	1		Media side lane assignment advertising for AppSel code 1
Page01 177(B1h)	0x11	17		Media side lane assignment advertising for AppSel code 2
Page01 178 (B2h)	0x01	1		Media side lane assignment advertising for AppSel code 3
Page01 179 (B3h)	0x11	17		Media side lane assignment advertising for AppSel code 4
Page01 180 (B4h)	0xff	255		Media side lane assignment advertising for AppSel code 5
Page01 181 (B5h)	0xff	255		Media side lane assignment advertising for AppSel code 6
Page01 182 (B6h)	0x01	1		Media side lane assignment advertising for AppSel code 7
Page01 183 (B7h)	0x01	1		Media side lane assignment advertising for AppSel code 8
Page01 184 (B8h)	0xFF	255		Media side lane assignment advertising for AppSel code 9
Page01 185 (B9h)	0xFF	255		Media side lane assignment advertising for AppSel code 10
Page01 186 (BAh)	0x01	1		Media side lane assignment advertising for AppSel code 11
Page01 187 (BBh)	0x11	17		Media side lane assignment advertising for AppSel code 12
Page01 188 (BCh)	0x00	0		Media side lane assignment advertising for AppSel code 13

Page01 189 (BDh)	0x00	0		Media side lane assignment advertising for AppSel code 14
Page01 190 (BEh)	0x00	0		Media side lane assignment advertising for AppSel code 15
Page01 191-222 (BFh–DEh)	0x00	0		Not Implemented
Page01 223 (DFh)	0x4B	75		Host Interface ID AppSel code 9
Page01 224 (E0h)	0xBF	191		Media Interface ID AppSel code 9
Page01 225 (E1h)	0x11	17		Host and Media Lane Count AppSel code 9
Page01 226 (E2h)	0xFF	255		Host Lane Assignment Options AppSel code 9
Page01 227 (E3h)	0x4C	76		Host Interface ID AppSel code 10
Page01 228 (E4h)	0xBF	191		Media Interface ID AppSel code 10
Page01 229 (E5h)	0x11	17		Host and Media Lane Count AppSel code 10
Page01 230 (E6h)	0xFF	255		Host Lane Assignment Options AppSel code 10
Page01 231 (E7h)	0x11	17		Host Interface ID AppSel code 11
Page01 232 (E8h)	0xBF	191		Media Interface ID AppSel code 11
Page01 233 (E9h)	0x88	136		Host and Media Lane Count AppSel code 11
Page01 234 (EAh)	0x01	1		Host Lane Assignment Options AppSel code 11
Page01 235 (EBh)	0xC0	192		Host Interface ID AppSel code 12
Page01 236 (ECh)	0xC0	192		Media Interface ID AppSel code 12
Page01 237 (EDh)	0x88	136		Host and Media Lane Count AppSel code 12
Page01 238 (EEh)	0x11	17		Host Lane Assignment Options AppSel code 12
Page01 239 (EFh)	0xFF	255		End of application
Page01 240-254 (F0h-FEh)	0x00	0		Not Implemented
Page01 255 (FFh)				Checksum
Page02 128(80h)	0x64	100		Temperature monitor high alarm threshold MSB
Page02 129(81h)	0x00	0		Temperature monitor high alarm threshold LSB
Page02 130(82h)	0xFB	251		Temperature monitor low alarm threshold MSB
Page02 131(83h)	0x00	0		Temperature monitor low alarm threshold LSB
Page02 132(84h)	0x5F	95		Temperature monitor high warning threshold MSB
Page02 133(85h)	0x00	0		Temperature monitor high warning threshold LSB
Page02 134(86h)	0x00	0		Temperature monitor low warning threshold MSB
Page02 135(87h)	0x00	0		Temperature monitor low warning threshold LSB
Page02 136(88h)	0x8C	140	î	Supply 3.3-volt monitor high alarm threshold MSB
Page02 137(89h)	0xA0	160	á	Supply 3.3-volt monitor high alarm threshold LSB
Page02 138(8Ah)	0x75	117	u	Supply 3.3-volt monitor low alarm threshold MSB
Page02 139(8Bh)	0x30	48	0	Supply 3.3-volt monitor low alarm threshold LSB
Page02 140(8Ch)	0x8A	138	è	Supply 3.3-volt monitor high warning threshold MSB
Page02 141(8Dh)	0xAC	172	¼	Supply 3.3-volt monitor high warning threshold LSB
Page02 142(8Eh)	0x77	119	W	Supply 3.3-volt monitor low warning threshold MSB

Page02 143(8Fh)	0x24	36	$	Supply 3.3-volt monitor low warning threshold LSB
Page02 144-167 (90h-A7h)	0x00	0		Not Implemented
Page02 168 (A8h)	0x50	80		Custom Monitor High Alarm Threshold LSB
Page02 169 (A9h)	0x00	0		Custom Monitor High Alarm Threshold MSB
Page02 170 (AAh)	0x00	0		Custom Monitor Low Alarm Threshold LSB
Page02 171 (ABh)	0x00	0		Custom Monitor Low Alarm Threshold MSB
Page02 172 (ACh)	0x4B	0		Custom Monitor High Warning Threshold LSB
Page02 173 (ADh)	0x00	0		Custom Mon High Warning Threshold MSB
Page02 174 (AEh)	0x05	5		Custom Monitor Low Warning Threshold LSB
Page02 175 (AFh)	0x00	0		Custom Monitor Low Warning Threshold MSB
Page02 176-254 (B0h-FEh)	0x00	0		
Page02 255(FFh)				Checksum
Page03 128-131(80h-83h)	0x00	0		User EEPROM
Page03 132(84h)	0x00	0		Insertion Counter MSB
Page03 133(85h)	0x00	0		Insertion Counter LSB
Page03 134(86h)	0x66	102		Cut-Off temperature
Page03 135(87h)	0x00	0		Power Spots control register
Page03 136(88h)	0x00	0		DSP Controller
Page03 137(89h)	0x00	0		Power Mode Select
Page03 138(8Ah)	0x00	0		PWM Power Control / Spot Enable
Page03 139(8Bh)	0x00	0		Digital Status of the low-speed signals.
Page03 140(8Ch)	0x00	0		Digital Control of Int signal
Page03 141(8Dh)	0x00	0		
Page03 142(8Eh)	0x00	0		
Page03 143(8Fh)	0x00	0		Internally measured Temperature T.S.2 MSB
Page03 144(90h)	0x00	0		Internally measured Temperature T.S.2 LSB
Page03 145-169(8Fh-A9h)	0x00	0		DSP internal debugging registers
Page03 170-179(AAh-B3h)	0x00	0		User EEPROM
Page03 180(B4h)	0x00	0		LT enable/disable
Page03 181-255(B5h-FFh)	0x00	0		User EEPROM

3.2.4 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-30	RO
	31-34	RW (VR)
	35-117	RO
	118-125	WO/SC
	126	RO
	126-127	RW (VR)
Page 00h	128-222	RO
	223-255	RW (NVR)
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03h	128-131	RW (NVR)
	132-133	RO
	134-137	RW (NVR)
	139	RO
	140-142	RW (NVR)
	143-169	RO
	170-255	RW (NVR)
Page 10h	128-129	RW(VR)
	131-136	RO
	137-138	RW(VR)
	139-142	R0
	143-144	WO
	145-152	RW(VR)
	153-161	RO
	162-173	RW(VR)
	174-212	RO
	213	RW(VR)
	214	R0
	215-216	RW(VR)
	217-255	RO
Page 11h	128-133	RO
	134	RO(COR)
	135-255	RO
Page 13h	128-143	RO
	144-175	RW (VR)
	176	RO
	177	RW (VR)

	178	RO
	179-255	RW VR
Page 14h	128	RW (NVR)
	129-255	RO (VR)
Page B0h – B8h	128-255	RW (NVR)

3.2.5 Password Protected Space

The memory space protected by password is RO, and can be written after successful password entry.

Password should be entered in Registers 122 to 125 (4 bytes) in low memory.
The default password is (in hex): 00 00 10 11.

The password can be changed in Registers 118 to 121.

Address	Bits	Name	Description	Type
118 – 121	7-0	Password Change Entry Area		WO
122 – 125	7-0	Password Entry Area		WO

The registers protected by Password are listed in the following table:

Page	Address	Description
Low Memory	1-2	Management Characteristics
	27-30	MciSpeedConfiguration Reserved and Custom
	35-36	Reserved and Custom
	42-84	Miscellaneous Status Information Extended Module Information
	118-121	Password Change
Page 00	129-221	Vendor Name, OUI, PN, Rev, SN, Date Code, CLEI Code, Power Characteristics Connector, Cable and Interface Information
Page 01	132-175	Durations Advertisements Module Characteristics Advertisement Module Supported Features
	191-222	Custom
	251-254	Miscellaneous Advertisements
Page 02	128-254	Alarm thresholds

3.3 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- INT/RSTn
- LPW/PRSn

3.3.1 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.
Reset is an active low signal on the host which is translated to an active low signal on the module.
Interrupt is an active high signal on the module which gets translated to an active low signal on the host.

3.3.2 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.
Low Power mode is an active low signal on the host which gets converted to an active low signal on the module.
Module Present is controlled by a pull-down resistor on the module which gets converted to an active low logic signal on the host.

3.4 ML4064-AL7I/R-224 Specific Functions

3.4.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4064-AL7I/R-224** implements two module states: ModuleLowPwr and ModuleReady.

The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the Module is in Low Power mode. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

3.4.2 Module State Transition

The state transition between Module Low Power and Module Ready is related to three parameters:

1. LowPwrRequestSW bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwrAllowRequestHW bit – software control, register 26 bit 6
3. LPWn – Hardware signal

According to these parameters, the state of the module is defined. Conditions for low-power state and ready state are summarized in the table below.

LowPwrRequestSW (Reg 26 bit 4)	LowPwrAllowRequestHW (register 24 bit 6)	LPWn	State
1	X	X	Module Low Pwr
0	1	0	Module Low Pwr
0	1	1	Module Ready
0	0	x	Module Ready

3.4.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Address	Bit	Name	Description	Type
26 (Lower Page)	6	LowPwrAllowRequestHW	Parameter used to control the module power mode (refer to section 3.4.2) Default value =1	RW
	4	LowPwrRequestSW	0b = high power mode (default) 1b =Forces module into low power mode	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit is self-clearing. 0b = not in reset 1b = Software reset	
3 (Lower Page)	0	Software Interrupt	Digital state of Interrupt: 0b = Interrupt source is present 1b = No interrupt source present	RO

3.4.4 Temperature Monitor

The **ML4064-AL7I/R-224** has 2 temperature sensors on the PCBA to continuously monitor the module temperature. In addition to one temperature monitor for the transceiver chip. Internally measured Module temperatures are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127°C to +128°C that is considered valid between –40° and +125° C.

Address	Bit	Name	Description	Type
14 Lower Page	All	Temperature MSB	Case Temperature	RO
15 Lower Page	All	Temperature LSB		
143 Page 03h	All	Temperature MSB	Internally measured TempSense 2 (PCB Bottom)	
144 Page 03h	All	Temperature LSB		
24 Lower Page	All	Temperature MSB	Internally measured DSP temperature	
25 Lower Page	All	Temperature LSB		

The distribution of internal temperature sensors is shown in the figures below:

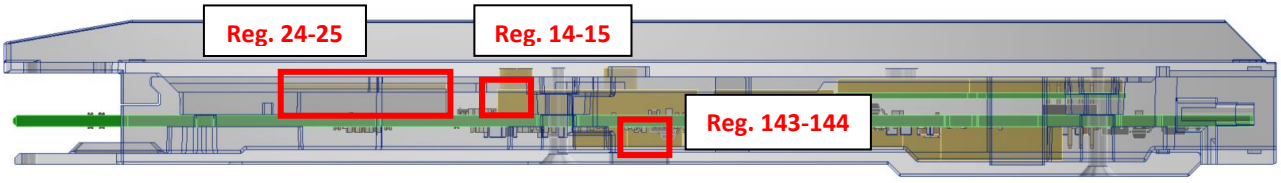


Figure 5: ML4064-AL7I-224 Temperature sensors location

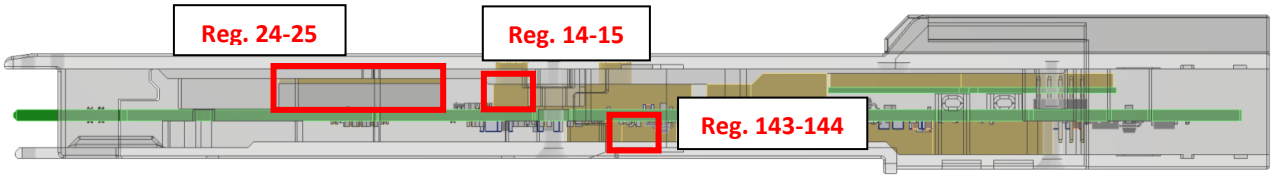


Figure 6: ML4064-AL7R-224 Temperature sensors location

The temperature alarms and warnings interrupt flags exist in lower page registers 9 and 11.

Address	Bit	Name	Description	Type
9 (Lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag	RO
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	

Address	Bit	Name	Description	Type
11 (Lower Page)	3	L-Temp Low Warning (DSP temp)	Latched low DSP temperature warning flag	RO
	2	L-Temp High Warning (DSP temp)	Latched high DSP temperature warning flag	
	1	L-Temp Low Alarm (DSP temp)	Latched low DSP temperature alarm flag	
	0	L-Temp High Alarm (DSP temp)	Latched high DSP temperature alarm flag	

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

3.4.5 Voltage Sense

A voltage sense circuit is available in the **ML4064-AL7I/R-224** that allows to measure the internal module supplied voltage VCC, with LSB unit is 0.1 mV.

Address	Bit	Name	Description	Type
16	All	Supply voltage MSB	Internally measured supply voltage	RO
17	All	Supply voltage LSB	Internally measured supply voltage	

The Voltage alarms and warnings interrupt flags exist in lower page.

Address	Bit	Name	Description	Type
9 (Lower Page)	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag	

3.4.6 Current Sense

A current sense circuit is available in the **ML4064-AL7I/R-224** that allows monitoring the current consumption. The current is stored in registers 18-19 of lower page.

The current sense is able to measure up to 15 A, with LSB unit of 1 mA.

Address	Bit	Name	Description	Type
18 (Lower Page)	All	Current Consumption MSB	Current consumption in mA	RO
19 (Lower Page)	All	Current Consumption LSB		

3.4.7 Maximum Power Indicator

The maximum power in the module is indicated by reading register 201 of Page 00.

Address	Bit	Name	Description	Default	Type
201 (Page 00)	All	Max Power Indicator	Module Maximum Power Consumption	Decimal: 172 corresponding to 43W	RO

3.4.8 Programmable Power Dissipation and Thermal Emulation

The **ML4064-AL7I/R-224** has a maximum power of 43W distributed between the DSP (14.5W) and the programmable power spots (28.5W).

The module's DSP and components normally consume 10.5W when in high power mode and DSP is locked to all host side lanes, an additional 4W can be added to the DSP power consumption when needed using register 136 (Page 03).

Address	Bit	Name	Description	Type
136 (Page03)	7:0	DSP Controller	**0x00**: additional DSP power **disabled** (default); the DSP power is 10.5W if all channels are locked. **0x01**: 4W additional DSP power **enabled.**	RW (NVR)

The programmable power spots are implemented on both the main PCBA (paddle card) and the daughter card, enabling flexible thermal emulation profiles depending on the selected operating mode.

Figure 7 (IHS option) and Figure 8 (RHS option) below show a side view of the distribution of Thermal Interface used to allow the heat conduction from the PCB to the shell. The yellow shapes represent the TIM.

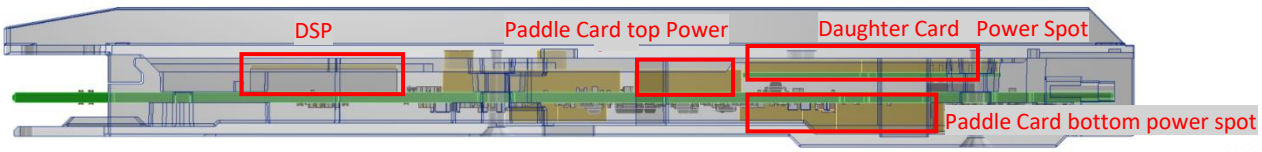


Figure 7: ML4064-AL7I-224 Thermal Interfaces Distribution

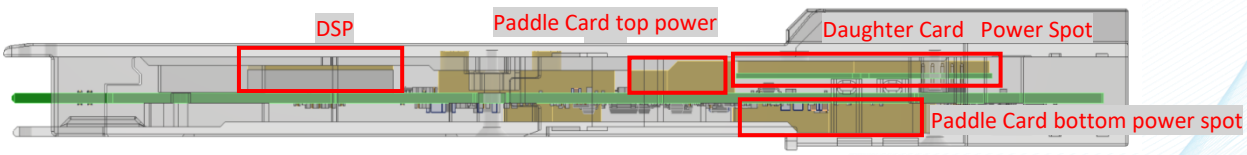


Figure 8: ML4064-AL7R-224 Thermal Interfaces Distribution

The power distribution (DSP and power spots) is shown in the image below (Figure 9).

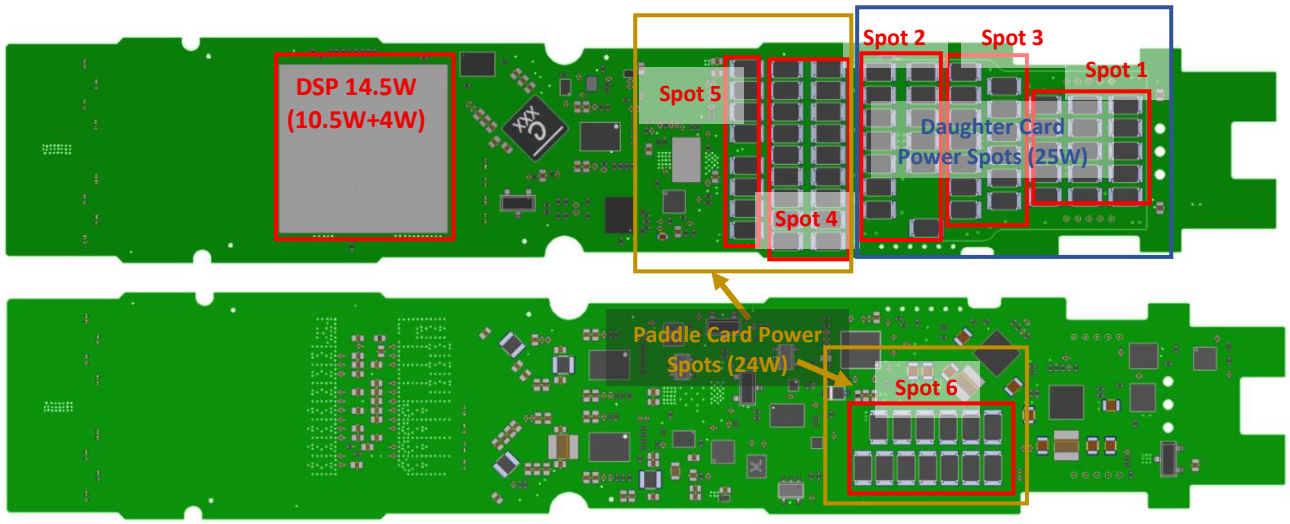


Figure 9: Thermal spots distribution

To provide flexible control while maintaining backward compatibility with previous hardware revisions, 4 power control modes are supported. The desired mode is selected using Register 137 (Page 03).
The power control mode determines how programmable power spots are managed and which registers are used for control.

Address	Bit	Name	Description		Value	Type
137 (Page03)	7:0	Power Mode Select	**Selects the programmable power control mode:**	**Related Power Spots**		RW (NVR)
			- Mode 1: Backward-Compatible Mode (Default)	Daughter Card only	0x00	
			- Mode 2: Power Spots on Paddle Card Mode	Paddle Card Spots (Spots 4, 5, 6) + Spot 2 (daughter card)	0x01	
			- Mode 3: Extended Daughter Card Mode	Daughter Card Spots (1, 2, 3) + Spot 5 (paddle card)	0x02	
			- Mode 4: Spot Selection Mode (On/Off Control)	Spots 1-6	0x03	

3.4.8.1 Mode 1 – Backward Compatible Mode (Default)

This mode maintains full backward compatibility with HW RevA.
In this mode, programmable power spots are enabled **only on the daughter card**, similar to the previous hardware revision.

The power spots are shown in the image below (Figure 10).

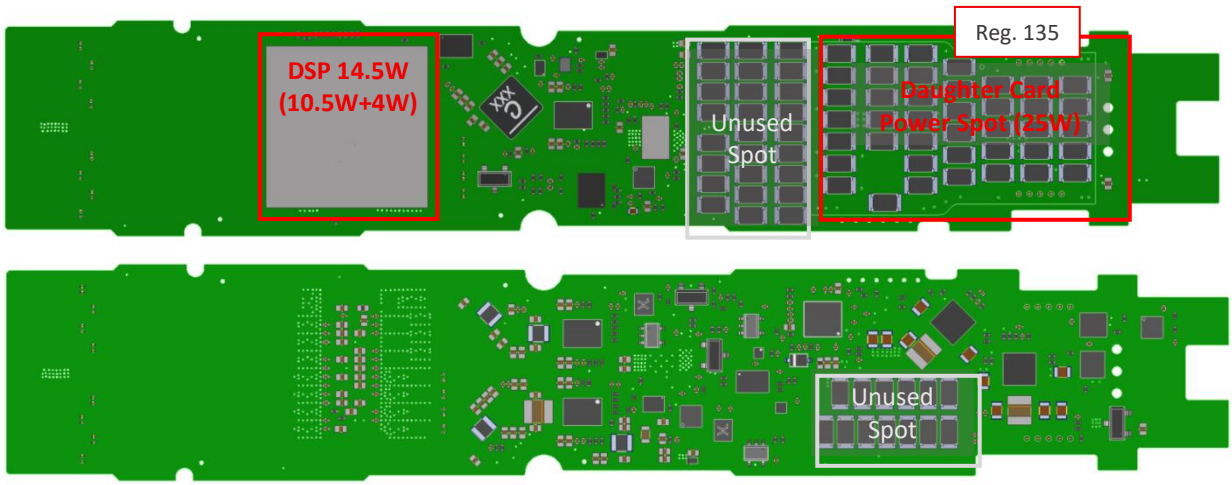


Figure 10: Power spots distribution (Mode 1)

The total max power in this mode would be 39.5W consisting of up to 25W of programmable power (from the entire daughter card only) and up to 14.5W of DSP power (including the additional 4W when enabled).

The daughter card power control is linear and performed through **Register 135 (Page 03)**. The power level is proportional to the register value:

$$PWR = Max\_Power \times \frac{Register\_Value}{255}$$

Where: **Max_Power ≈ 25W** (daughter card maximum power).

A value of 0 written on the power spot register will turns off the power spot, and a value of 255 sets it to maximum power dissipation.

Address	Bit	Name	Description	Type
135 (Page03)	7:0	Power Controller	Controls daughter card power spot. Programmable power consumption up to 25W (daughter card)	RW (NVR)
136 (Page03)	7:0	DSP Controller	**0x00**: additional DSP power **disabled** (default); the DSP power is 10.5W if all channels are locked. **0x01**: 4W additional DSP power **enabled.**	RW (NVR)

Example values for Register 135:

Register Value	Programmed Power Level
0xFF	~25W (maximum power)
0x7F	~12.5W (half power)
0x00	Power spot disabled

3.4.8.2 Mode 2 – Power Spots on Paddle Card

In this mode, programmable power spots located on the **paddle card (PCBA)** can be enabled. The paddle card power is controlled linearly using **Register 135 (Page 03)** with a maximum programmable power of **24W**.
In addition, daughter card power spot (Spot 2) may still be enabled using PWM-based control, allowing up to **5W** of additional power.
The PWM power level is directly configured in watts through **Register 138 (Page 03)**, with LSB unit of 0.5W.

The power spots are shown in the image below (Figure 11).

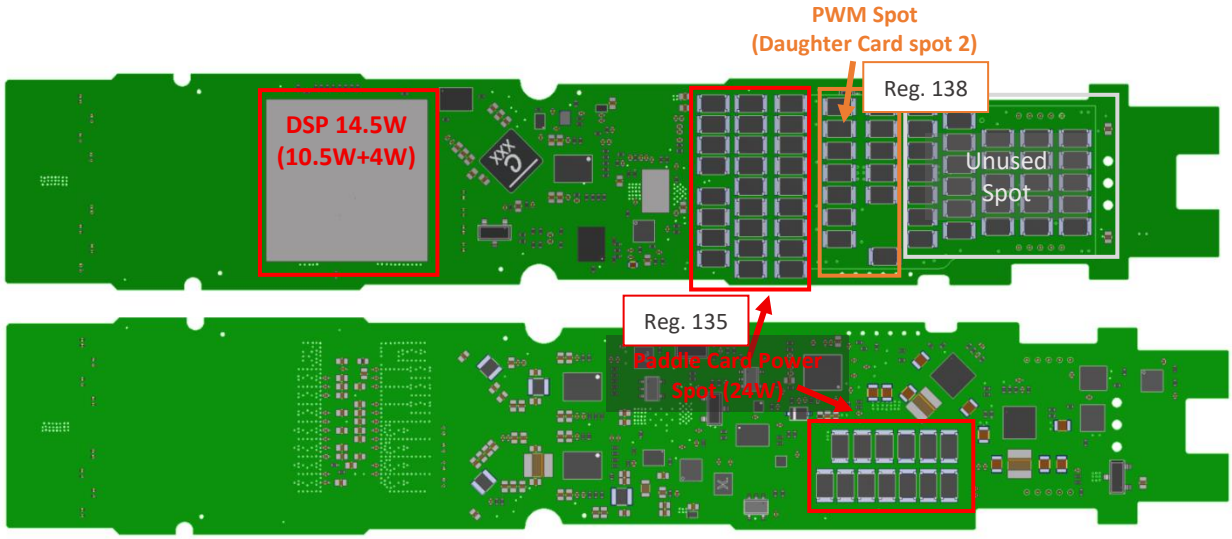


Figure 11: Power spots distribution (Mode 2)

The total max power in this mode is 43W, consisting of up to 24W of programmable power from all the paddle card spots, up to 5W from the daughter card (spot 2), and up to 14.5W of DSP power (including the additional 4W when enabled).

Address	Bit	Name	Description	Type
135 (Page03)	7:0	Power Controller	Controls the paddle card (PCBA) power spot. Programmable power consumption up to 24W (Paddle Card).	RW (NVR)
138 (Page03)	7:0	PWM Power Control	Controls additional daughter card power (spot 2), up to 5W. LSB unit is 0.5W	RW (NVR)
136 (Page03)	7:0	DSP Controller	**0x00**: additional DSP power **disabled** (default); the DSP power is 10.5W if all channels are locked. **0x01**: 4W additional DSP power **enabled.**	RW (NVR)

3.4.8.3 Mode 3 – Extended Daughter Card Mode

This mode operates similarly to Mode 1, with daughter card power spots controlled linearly through **Register 135 (Page 03)**.
Additionally, PWM-based fine power control is available through **Register 138 (Page 03)**, with LSB unit of 0.5W, allowing an additional programmable power of up to **4W** on the Paddle Card power spot (Spot 5).

The power spots are shown in the image below (Figure 12).

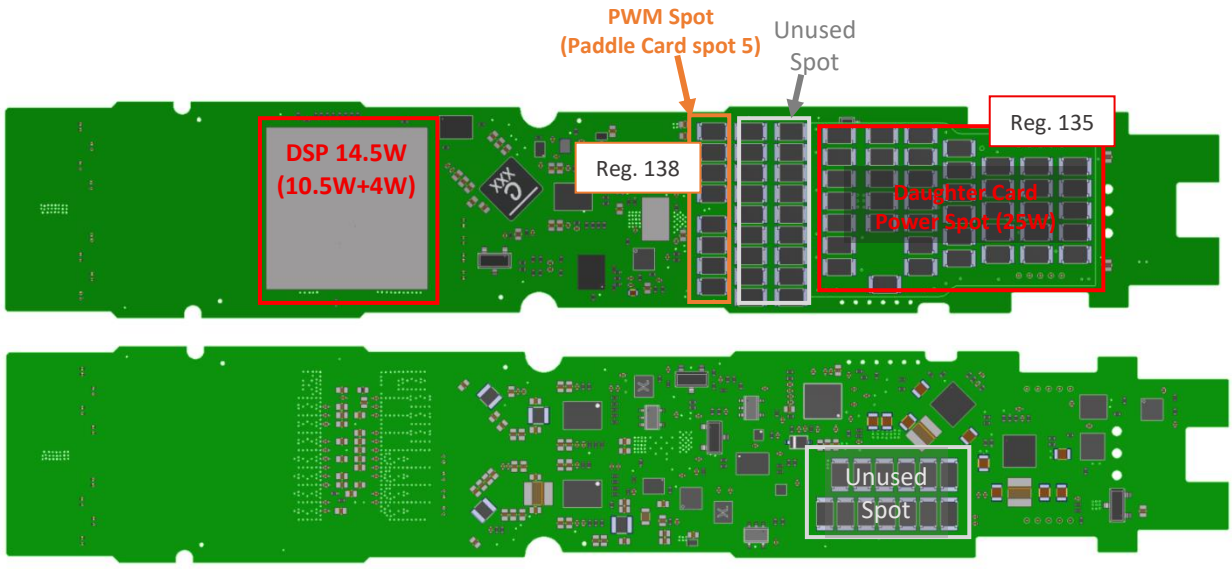


Figure 12: Power spots distribution (Mode 3)

The total max power in this mode is 43W, consisting of up to 25W of programmable power from the entire daughter card, up to 4W from the paddle card (spot 5), and up to 14.5W of DSP power (including the additional 4 W when enabled).

Address	Bit	Name	Description	Type
135 (Page03)	7:0	Power Controller	Controls daughter card power spot. Programmable power consumption up to 25W (daughter card)	RW (NVR)
138 (Page03)	7:0	PWM Power Control	Controls the additional paddle card power (spot 5) up to 4W. LSB unit is 0.5W	RW (NVR)
136 (Page03)	7:0	DSP Controller	**0x00**: additional DSP power **disabled** (default); the DSP power is 10.5W if all channels are locked. **0x01**: 4W additional DSP power **enabled.**	RW (NVR)

3.4.8.4 Mode 4 – Spot Selection Mode (On/Off Control)

In this mode, all available power spots operate in binary on/off mode. The user directly selects which spots are enabled.

The module contains 6 independent power spots, controlled through **Register 138 (Page 03)**.

The power spots are shown in the image below (Figure 13).

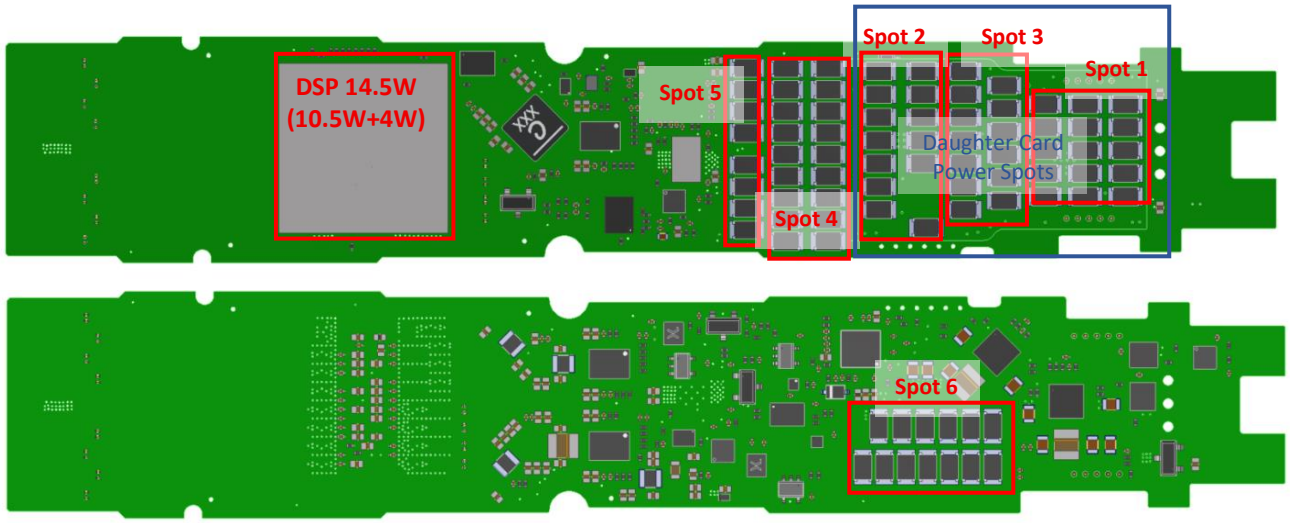


Figure 13: Power spots distribution (Mode 4)

The total max power in this mode is 43W, consisting the power from selected power spots on the paddle card (PCBA) and daughter card, and up to 14.5W of DSP power (including the additional 4W when enabled).

The 6 power spots, controlled through Register 138 (Page 03), with each bit corresponding to one power spot:

Address	Bit	Name	Description	Power Value	Type
138 (Page 03)	0	Spot Enable	Enable Spot 1 (daughter card)	9W	RW (NVR)
	1		Enable Spot 2 (daughter card)	8W	
	2		Enable Spot 3 (daughter card)	8W	
	3		Enable Spot 4 (paddle card)	11W	
	4		Enable Spot 5 (paddle card)	5W	
	5		Enable Spot 6 (paddle card)	8W	

Note: If the user enables a combination of spots that would exceed the maximum allowed module power, the module firmware automatically clears the corresponding bits to ensure that the total power dissipation remains within the allowed limit.

Address	Bit	Name	Description	Type
136 (Page03)	7:0	DSP Controller	**0x00**: additional DSP power **disabled** (default); the DSP power is 10.5W if all channels are locked. **0x01**: 4W additional DSP power **enabled.**	RW (NVR)

3.4.8.5 Power Control Registers Summary

The functions of the power control registers are summarized in the table below.

Page	Address	Bit	Name	Description	Type
Page 03	135	7:0	Power Controller	Linear power control for daughter card (Modes 1 & 3) or paddle card (Mode 2)	RW (NVR)
	136	7:0	DSP Controller	0x00: Additional DSP power disabled 0x01: Enable additional 4W DSP power	
	137	7:0	Power Mode Select	Selects the power control mode (Mode 1–4)	
	138	7:0	PWM Power Control	Configures PWM-based power in watts (Modes 2 & 3)	
	138	5:0	Spot Enable	On/Off control for the six power spots (Mode 4)	

3.4.8.6 Example

This example shows how to configure the module to emulate a total power of ~30W by distributing the power between the DSP, daughter card power, and paddle card power spot (PWM-controlled), using mode 3.

Thus, the target power distribution, using power mode 3, can be as follows:

- DSP base power: ~10.5W
- Additional DSP power: 4W
- Daughter card power spot: 12W
- Paddle card PWM power spot: 3.5W

➔ Total = 30W.

The user should then:

1. Select Mode 3: Write 0x02 to Register 137 (Page 03).
2. Enable additional DSP power: Write 0x01 to Register 136 (Page 03).
3. Program 12W from the daughter card power spot (Max_Power =25W):
   $PWR = Max\_Power \times \frac{Register\_Value}{255}$; → $Register\_Value = \frac{12}{25} \times 255 \approx 122$
   → Write 0x7A (122 decimal) to Register 135 (Page 03).
4. Program 3.5W from the paddle card power spot (resolution=0.5W per LSB, and max=4W):
   → Write 0x07 to Register 138 of Page 03 (Reg 138= 3.5/0.5=7=0x07).

3.4.9 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined to 102°C.
The module is continuously monitoring the DSP and case temperatures and checking their value against the Cut-Off temperature. Once any of these temperatures reaches the cut-off value, the DSP will automatically switch to Low Power mode in order to prevent overheating (which will also prevent DSP temperature reading). Once the case temperature is 5 degrees below cut-off value, the DSP goes back to its previous state.
The **ML4064-AL7I/R-224** cut-off is set to a temperature of 102°C by default, and can be programmed from register 134 of memory page 03 to any value below 102°C which is the maximum Cut-Off temperature.

Address	Bit	Name	Description	Type
134	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1°C (Default: 102°C)	RW (NVR)

3.4.10 Insertion Counter

The Insertion Counter contains the number of times the module was hot plugged into a host port. The counter will be updated only upon physical insertion to a port. Power cycling while in a port or module soft reset will not increment the counter.
The Insertion Counter can be read from registers 132-133 page 03.

Address	Bit	Name	Description	Type
132 (page 03)	MSB	Power Cycle Counter MSB		RO
133 (page 03)	LSB	Power Cycle Counter LSB	LSB unit = 1 initializing sequence	

3.4.11 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow you to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Default Value	Type
128 (page 02)	ALL	High temp alarm threshold (MSB)	100˚C	RO
129 (page 02)	ALL	High temp alarm threshold (LSB)		
130 (page 02)	ALL	Low temp alarm threshold (MSB)	-5° C	
131 (page 02)	ALL	Low temp alarm threshold (LSB)		
132 (page 02)	ALL	High temp warning threshold (MSB)	95˚C	
133 (page 02)	ALL	High temp warning threshold (LSB)		
134 (page 02)	ALL	Low temp warning threshold (MSB)	0˚C	

135 (page 02)	ALL	Low temp warning threshold (LSB)		
136 (page 02)	ALL	High volt alarm threshold (MSB)	3.6 V	
137 (page 02)	ALL	High volt alarm threshold (LSB)		
138 (page 02)	ALL	Low volt alarm threshold (MSB)	3.0 V	
139 (page 02)	ALL	Low volt alarm threshold (LSB)		
140 (page 02)	ALL	High volt warning threshold (MSB)	3.55 V	
141 (page 02)	ALL	High volt warning threshold (LSB)		
142 (page 02)	ALL	Low volt warning threshold (MSB)	3.05 V	
143 (page 02)	ALL	Low volt warning threshold (LSB)		

3.4.12 Low Speed Signals Pin Status

The register below is accessed from page 03h.

Address	Page	Bit	Name	Description	Type
139	Page03	1	LPWn logic status	Read 1b: High Read 0b: Low	RO

3.4.13 INT Control

During power-up of the module, INT is defaulted to negated. Afterward, host can set the status of this indicator to any status through an I2C registers **in Upper Page 03**. Setting it should not affect any operation in the module.

Address	Page	Bit	Name	Description	Type
140	Page 03	1:0	INT Control	Digital Control of INT: 0x: Normal Operation 10: Force M_INT to logic 0 11: Force the M_INT to logic 1	RW

In “Normal Operation”, INT is asserted when either of these states occurs:

- High/low alarm/warning for temperature
- High/low alarm/warning for voltage
- module state machine state change
- data path state machine state change
- LOS, CDR LOL or RXOUT status change
- Module firmware error flag set
- CDB command complete

4 High Speed

The **ML4064-AL7I/R-224** includes a low power 1600G retimer transceiver chip. The transceiver operates at 106.25 PAM4, Gray coded pattern. The default mode of operation is the retimed loopback mode.

4.1 Supported Rates

Application Bit Rate, Gb/s[2]	Lane Count	Lane Signaling Rate, GBd[2]	Modulation	AppSel Code	Application
212.50	1	106.25	PAM4	1	200GAUI-1 (Annex176E)
425.00	2	106.25	PAM4	2	400GAUI-2 (Annex176E)
850.00	4	106.25	PAM4	3	800GAUI-4 (Annex176E)
1700.00	8	106.25	PAM4	4	1.6TAUI-8 (Annex176E)
850.00	8	53.125	PAM4	5	800GAUI-8 S C2M (Annex 120G)
850.00	8	53.125	PAM4	6	800GAUI-8 L C2M (Annex 120G)
425.00	4	53.125	PAM4	7	400GAUI-4-S C2M (Annex 120G)
425.00	4	53.125	PAM4	8	400GAUI-4-L C2M (Annex 120G)
106.25	1	53.125	PAM4	9	100GAUI-1-S C2M (Annex 120G)
106.25	1	53.125	PAM4	10	100GAUI-1-L C2M (Annex 120G)
53.13	1	26.5625	PAM4	11	50GAUI-1 C2M
1700.00	8	106.25	PAM4	12	Custom Application

4.2 Advertisement

4.2.1 Supported AppSel Codes

This paragraph lists the module supported AppSel codes:

Address	Name	Description	Default Value
LowMem 85	Media Type	The MediaType field defines the interpretation of MediaInterfaceID values in the following Application Descriptors. In this application it indicates "Active Cables"	0x04
LowMem 86	Host Interface ID AppSel code 1	200GAUI-1 (Annex176E)	0x80
LowMem 87	Media Interface ID AppSel code 1	Active Loopback module	0xBF
LowMem 88	Host and Media Lane Count AppSel code 1	1 host lane and 1 media lane	0x11
LowMem 89	Host Lane Assignment Options AppSel code 1	Application begins on all host lanes	0xFF
LowMem 90	Host Interface ID AppSel code 2	400GAUI-2 (Annex176E)	0x81
LowMem 91	Media Interface ID AppSel code 2	Active Loopback module	0xBF
LowMem 92	Host and Media Lane Count AppSel code 2	2 host lane and 2 media lane	0x22
LowMem 93	Host Lane Assignment Options AppSel code 2	Application begins on host lanes 1,3,5,7	0x55

LowMem 94	Host Interface ID AppSel code 3		800GAUI-4 (Annex176E)	0x82
LowMem 95	Media Interface ID AppSel code 3		Active Loopback module	0xBF
LowMem 96	Host and Media Lane Count AppSel code 3		4 host lanes and 4 media lane	0x44
LowMem 97	Host Lane Assignment Options AppSel code 3		Application begins on host lanes 1 and 5	0x11
LowMem 98	Host Interface ID AppSel code 4		1.6TAUI-8 (Annex176E)	0x83
LowMem 99	Media Interface ID AppSel code 4		Active Loopback module	0xBF
LowMem 100	Host and Media Lane Count AppSel code 4		8 host lanes and 8 media lanes	0x88
LowMem 101	Host Lane Assignment Options AppSel code 4		Application begins on host lane 1	0x01
LowMem 102	Host Interface ID AppSel code 5		800GAUI-8 S C2M (Annex 120G)	0x51
LowMem 103	Media Interface ID AppSel code 5		Active Loopback module	0xBF
LowMem 104	Host and Media Lane Count AppSel code 5		8 host lanes and 8 media lanes	0x88
LowMem 105	Host Lane Assignment Options AppSel code 5		Application begins on host lane 1	0x01
LowMem 106	Host Interface ID AppSel code 6		800GAUI-8 L C2M (Annex 120G)	0x52
LowMem 107	Media Interface ID AppSel code 6		Active Loopback module	0xBF
LowMem 108	Host and Media Lane Count AppSel code 6		8 host lanes and 8 media lanes	0x88
LowMem 109	Host Lane Assignment Options AppSel code 6		Application begins on host lane 1	0x01
LowMem 110	Host Interface ID AppSel code 7		400GAUI-4-S C2M (Annex 120G)	0x4F
LowMem 111	Media Interface ID AppSel code 7		Active Loopback module	0xBF
LowMem 112	Host and Media Lane Count AppSel code 7		4 host lanes and 4 media lanes	0x44
LowMem 113	Host Lane Assignment Options AppSel code 7		Application begins on host lanes 1 and 5	0x11
LowMem 114	Host Interface ID AppSel code 8		400GAUI-4-L C2M (Annex 120G)	0x50
LowMem 115	Media Interface ID AppSel code 8		Active Loopback module	0xBF
LowMem 116	Host and Media Lane Count AppSel code 8		4 host lanes and 4 media lanes	0x44
LowMem 117	Host Lane Assignment Options AppSel code 8		Application begins on host lanes 1 and 5	0x11
Page 01h 153	Bit 7	RxOutputLevel3Supported	0b/1b: Amplitude Code 3 not supported/supported	1
	Bit 6	RxOutputLevel2Supported	0b/1b: Amplitude Code 3 not supported/supported	1
	Bit 5	RxOutputLevel1Supported	0b/1b: Amplitude Code 3 not supported/supported	1
	Bit 4	RxOutputLevel0Supported	0b/1b: Amplitude Code 3 not supported/supported	1
Page 01h 154	Bit 7-4	RxOutputEqPostCursorMax	Maximum supported value of the Rx Output Eq Post-cursor control	0x7
	Bit 3-0	RxOutputEqPreCursorMax	Maximum supported value of the Rx Output Eq Pre-cursor control	0x7
Page 01h 162	Bit 4-3	RxOutputEqControlSupported	00b: Rx Output Eq control not supported 01b: Rx Output Eq Pre-cursor control supported 10b: Rx Output Eq Post-cursor control supported 11b: Rx Output Eq Pre- and Post-cursor control supported	11
	Bit 2	RxOutputAmplitudeControlSupported	0b: Rx Output Amplitude control not supported 1b: Rx Output Amplitude control supported	1
Page 01h 176	MediaLaneAssignmentOptionsApp1		Media Lane Assignment Options for the Application advertised in Application descriptor identified by AppSel <i>. Bits 0-7 form a bit map corresponding to Media Lanes 1-8. A set bit indicates that a Data Path for the	0xFF
Page 01h 177	MediaLaneAssignmentOptionsApp2			0x55
Page 01h 178	MediaLaneAssignmentOptionsApp3			0x11

Page 01h 179	MediaLaneAssignmentOptionsApp4	Application is allowed to begin on the corresponding Media Lane. Each instance of an Application uses contiguous Media Lane numbers. If multiple instances of a single Application are allowed, each starting point is identified, and all instance must be supported concurrently.	0x01
Page 01h 180	MediaLaneAssignmentOptionsApp5		0x01
Page 01h 181	MediaLaneAssignmentOptionsApp6		0x01
Page 01h 182	MediaLaneAssignmentOptionsApp7		0x11
Page 01h 183	MediaLaneAssignmentOptionsApp8		0x11
Page 01h 184	MediaLaneAssignmentOptionsApp9		0xFF
Page 01h 185	MediaLaneAssignmentOptionsApp10		0xFF
Page 01h 186	MediaLaneAssignmentOptionsApp11		0x00
Page 01h 223	Host Interface ID AppSel code 9	100GAUI-1-S C2M (Annex 120G)	0x4B
Page 01h 224	Media Interface ID AppSel code 9	Active Loopback module	0xBF
Page 01h 225	Host and Media Lane Count AppSel code 9	1 host lanes and 1 media lanes	0x11
Page 01h 226	Host Lane Assignment Options AppSel code 9	Application begins on all host lanes	0xFF
Page 01h 227	Host Interface ID AppSel code 10	100GAUI-1-L C2M (Annex 120G)	0x4C
Page 01h 228	Media Interface ID AppSel code 10	Active Loopback module	0xBF
Page 01h 229	Host and Media Lane Count AppSel code 10	1 host lanes and 1 media lanes	0x11
Page 01h 230	Host Lane Assignment Options AppSel code 10	Application begins on all host lanes	0xFF
Page 01h 231	Host Interface ID AppSel code 11	CAUI-4 C2M (Annex 83E) without FEC	0x11
Page 01h 232	Media Interface ID AppSel code 11	Active Loopback module	0xBF
Page 01h 233	Host and Media Lane Count AppSel code 11	4 host lanes and 4 media lanes	0x88
Page 01h 234	Host Lane Assignment Options AppSel code 11	Application begins on host lanes 1 and 5	0x01
Page 01h 235	Host Interface ID AppSel code 12	Custom application for long traces	0xC0
Page 01h 236	Media Interface ID AppSel code 12	Custom application for long traces	0xC0
Page 01h 237	Host and Media Lane Count AppSel code 12	8 host lanes and 8 media lanes	0x88
Page 01h 238	Host Lane Assignment Options AppSel code 12	1 host lanes and 1 media lanes	0x11
Page 01h 239	Terminating the AppSel codes	End of list	0xFF

4.2.2 Supported Features and Capabilities

This paragraph lists the module supported features and capabilities. All registers mentioned in the table below are present in page 13h.

Address	Bit	Name	Description	Default Value	Type
128	4	PerLaneHostSideLoopbacks	0b: Not supported 1b: Supported	0	RO
	3	HostSideInputLoopback	0b: Not supported 1b: Supported	1	
129	7-6	GatingSupport	0: Not Supported 1: Supported with time accuracy <= 2 ms 2: Supported with time accuracy <= 20 ms 3: Supported with time accuracy > 20 ms	0	RO
	5	GatingResultsSupported	Gating result statistics selectable by diagnosticsSelector (14h:128) values 11h-15h are: 0b: Not supported 1b: Supported	0	

	4	PeriodicUpdatesSupported	Realtime statistics selectable by DiagnosticsSelector (14h:128) values 01h-06h are periodically updated during measurement: 0b: no periodic update during measurement 1b: periodic update during measurement	1	
	3	PerLaneGatingTimersSupported	0b: Only two global gating timers are available for all lanes on all Banks, one for Host Side Measurements and one for Media Side Measurements. 1: Per lane gating timers are supported in all Banks	0	
	2	AutoRestartGatingSupported	0b: AutoRestartGating control (13h:177.4) not supported 1b: AutoRestartGating control (13h:177.4) supported	0	
130	4	HostSideInputSNRMeasurement	Indicates if hos side SNR measurement reported via Diagnostics Selection value 06h is supported (Byte 14h:128) 1b: Supported 0b: Not supported	1	RO
	1	BitsAndErrorsCountingSupported	Indicates if DiagnosticsSelector values 02h-05h are supported (Page 14h byte 128, Table 8-114) 0b: Not supported 1b: Supported	1	
131	2	PRBSGeneratorHostSidePostFEC	0b: Not supported 1b: Supported	1	RO
	1	PRBSCheckerHostSidePreFEC	0b: Not supported 1b: Supported	1	
132	7	HostSideGeneratorSupportsPattern7	PRBS-13 (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	0	RO
	6	HostSideGeneratorSupportsPattern6	PRBS-13Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	1	
	5	HostSideGeneratorSupportsPattern5	PRBS-15 (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	0	
	4	HostSideGeneratorSupportsPattern4	PRBS-15Q (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	1	
	3	HostSideGeneratorSupportsPattern3	PRBS-23 (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	0	
	2	HostSideGeneratorSupportsPattern2	PRBS-23Q (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	1	
	1	HostSideGeneratorSupportsPattern1	PRBS-31 (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsPattern0	PRBS-31Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	1	

133	7	HostSideGeneratorSupportsPattern15	User Pattern (Programmable pattern provided in Bytes 13h:224-255): 0b: Not supported 1b: Supported	1	RO
	6	HostSideGeneratorSupportsPattern14	Custom Vendor defined pattern	1	
	5	HostSideGeneratorSupportsPattern13	Reserved	0	
	4	HostSideGeneratorSupportsPattern12	SSPRQ (As defined in IEEE 802.3-2018 clause 120.5.11.2.3)	1	
	3	HostSideGeneratorSupportsPattern11	PRBS-7 (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	0	
	2	HostSideGeneratorSupportsPattern10	PRBS-7Q (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	1	
	1	HostSideGeneratorSupportsPattern9	PRBS-9 (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsPattern8	PRBS-9Q (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	1	
136	7	HostSideCheckerSupportsPattern7	PRBS-13 (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	0	RO
	6	HostSideCheckerSupportsPattern6	PRBS-13Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	1	
	5	HostSideCheckerSupportsPattern5	PRBS-15 (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	0	
	4	HostSideCheckerSupportsPattern4	PRBS-15Q (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	1	
	3	HostSideCheckerSupportsPattern3	PRBS-23 (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	0	
	2	HostSideCheckerSupportsPattern2	PRBS-23Q (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	1	
	1	HostSideCheckerSupportsPattern1	PRBS-31 (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	0	
	0	HostSideCheckerSupportsPattern0	PRBS-31Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	1	
137	7	HostSideCheckerSupportsPattern15	User Pattern (Programmable pattern provided in Bytes 13h:224-255): 0b: Not supported 1b: Supported	0	RO
	6	HostSideCheckerSupportsPattern14	Custom Vendor defined pattern	0	

	5	HostSideCheckerSupportsPattern13	Reserved	0	
	4	HostSideCheckerSupportsPattern12	SSPRQ (As defined in IEEE 802.3-2018 clause 120.5.11.2.3)	0	
	3	HostSideCheckerSupportsPattern11	PRBS-7 (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	0	
	2	HostSideCheckerSupportsPattern10	PRBS-7Q (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	1	
	1	HostSideCheckerSupportsPattern9	PRBS-9 (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	0	
	0	HostSideCheckerSupportsPattern8	PRBS-9Q (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	1	
140	7-6	RecoveredClockForGeneratorOptions	Options to use recovered clock for contra-directional pattern generator on the same module side: 00b: not supported 01b: supported without loopback 10b: supported with loopback 11b: supported with and without loopback	0b10	RO
	5	ReferenceClockForPatternsSupported	option to use reference clock for pattern generation: 0b: Not supported 1b: Supported	1	
	3-0	UserPatternLengthSupported	Maximum length L of the user defined pattern, where the field value n encodes L as L=2(n+1), i.e. 0000b: 2 bytes, …, 1111b: 32 bytes	0b0111	
141	3	HostSideCheckerSupportsDataSwap	Register 162 for swapping the MSB and LSB for PAM4 patterns: 0b: Not supported 1b: Supported	0	RO
	2	HostSideCheckerSupportsDataInvert	Register 161 for pattern inversion: 0b: Not supported 1b: Supported	0	
	1	HostSideGeneratorSupportsDataSwap	Register 146 for swapping the MSB and LSB for PAM4 patterns: 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsDataInvert	Register 145 for pattern inversion: 0b: Not supported 1b: Supported	0	
142	3	HostCheckerSupportsPerLaneEnable	Host Side pattern checker for lane i enabled in 13h:160 enables lane i 0b: per lane enable not supported 1b: per lane enable supported	1	RO
	2	HostCheckerSupportsPerLanePattern	Host Side pattern selection for checker 0b: Lane 1 Pattern Type 13h:164.3-0 is used for all lanes. 1b: Per lane Pattern selection 13h:164-167	1	
	1	HostGeneratorSupportsPerLaneEnable	Host Side pattern generator for lane i enabled in 13h:144 enables lane i	1	

			0b: per lane enable not supported 1b: per lane enable supported		
	0	HostGeneratorSupportsPerLanePattern	Host Side pattern selection for generator 0b: Lane 1 Pattern 13h:148.3-0 is used for all lanes. 1b: Per lane Pattern selection 13h.148-151	1	

4.3 Output Lane Status Indicator & Lane Flags

The LOS and CDR LOL are two indicators of the signal status received by the Host side TXIN. as per CMIS specs these indicators are reflected in registers 136 and 137 of page 11h.

The OutputStatusRx output status indication register describes the status of the high-speed outputs of a module. RX OUT signal valid flags can be read from register 132 page 11h. The signal on an Rx output host lane is declared valid in the OutputStatusRx register only while the module is actually sending a valid signal to the host.

Address	Bit	Name	Description	Default Value	Type
132	7	Output Status Rx8	0b: Output Signal invalid 1b: Output Signal Valid		RO
	6	Output Status Rx7			
	5	Output Status Rx6			
	4	Output Status Rx5			
	3	Output Status Rx4			
	2	Output Status Rx3			
	1	Output Status Rx2			
	0	Output Status Rx1			
136	7	LOS TX8	LOS FlagTx Latched Tx LOS Flag, host lane		RO
	6	LOS TX7			
	5	LOS TX6			
	4	LOS TX5			
	3	LOS TX4			
	2	LOS TX3			
	1	LOS TX2			
	0	LOS TX1			
137	7	CDR LOL TX8	CDR LOL Flag Tx Latched Tx CDR LOL Flag, host lane		RO
	6	CDR LOL TX8			
	5	CDR LOL TX8			
	4	CDR LOL TX8			
	3	CDR LOL TX8			
	2	CDR LOL TX8			
	1	CDR LOL TX8			
	0	CDR LOL TX8			

4.4 PRBS Generator

The Pattern Generator control is described in this section. The generated pattern is transmitted from the module to the host on the RX electrical output. The PRBS generator control registers are present in Page 13h. the PRBS generator mode is enabled automatically when the Loopback mode is disabled.

Address	Bit	Name	Description	Default Value	Type
144	7	HostSideGeneratorEnableLane8	0b: Disable pattern generator 1b: Enable pattern generator	0	RW (VR)
	6	HostSideGeneratorEnableLane7		0	
	5	HostSideGeneratorEnableLane6		0	
	4	HostSideGeneratorEnableLane5		0	
	3	HostSideGeneratorEnableLane4		0	
	2	HostSideGeneratorEnableLane3		0	
	1	HostSideGeneratorEnableLane2		0	
	0	HostSideGeneratorEnableLane1		0	
148	7-4	HostSideGeneratorPatternSelectLane2	The Pattern IDs are summarized below: 0: PRBS-31Q 1: PRBS-31 2: PRBS-23Q 3: PRBS-23 4: PRBS-15Q 5: PRBS-15 6: PRBS-13Q 7: PRBS-13 8: PRBS-9Q 9: PRBS-9 10: PRBS-7Q 11: PRBS-7 12: SSPRQ 13: Reserved 14: Custom 15: User Pattern	0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane1		0x0	
149	7-4	HostSideGeneratorPatternSelectLane4		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane3		0x0	
150	7-4	HostSideGeneratorPatternSelectLane6		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane5		0x0	
151	7-4	HostSideGeneratorPatternSelectLane8		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane7		0x0	
176	7-4	HostPRBSGeneratorClockSource	0: All lanes uses Internal Clock 1: All lanes uses Recovered Clock Media Lane 1 2: All lanes uses Recovered Clock Media Lane 2 3: All lanes uses Recovered Clock Media Lane 3 4: All lanes uses Recovered Clock Media Lane 4 5: All lanes uses Recovered Clock Media Lane 5 6: All lanes uses Recovered Clock Media Lane 6 7: All lanes uses Recovered Clock Media Lane 7 8: All lanes uses Recovered Clock Media Lane 8 Ah-Eh: Reserved	0b1111	RO (VR)

			Fh: Recovered clock from Respective Media Lane/Datapaths are used		
224-239	7-0	UserPattern	Host defined user pattern (16 Bytes)	- First 8 bytes: 0xFF - Last 8 bytes: 0x00	RW (VR)

4.5 PRBS Checker

The pattern Checker control is described in this section. The control is applied on the host side of the module for data received at the TX electrical input. The PRBS checker control registers are present in Page 13h. the PRBS checker mode is enabled by default.

The PRBS checker behavior described in this section is for the un-gated mode (13h:177.3-1 = 000b). In this mode, the error metrics measurement runs continuously. When the host enables the disabled PRBS checkers (register 160 in the table below) all error counters for the enabled lanes are cleared and then start accumulating. When the host disables enabled PRBS checkers (register 160 in the table below) error counting is stopped, and error counting results will be available via Selector 01-05h.
The error information availability is related to the PeriodicUpdatesSupported settings (13h:129.4):

- 13h:129.4 = 0: real time error information is not updated and error information is only available when the error counting is stopped by checker disable
- 13h:129.4 = 1: real time error information is available with Selectors 01-05h. Update period is configured by 13h:177.0, as described in section 4.8.1.

The error counters and restart accumulation are controlled form ResetErrorInformation control bit 13h:177.5, as described in section 4.8.1.

Address	Bit	Name	Description	Default Value	Type
160	7	HostSideCheckerEnableLane8	0b: Disable pattern Checker 1b: Enable pattern Checker	1	RW (VR)
	6	HostSideCheckerEnableLane7		1	
	5	HostSideCheckerEnableLan6		1	
	4	HostSideCheckerEnableLane5		1	
	3	HostSideCheckerEnableLane4		1	
	2	HostSideCheckerEnableLane3		1	
	1	HostSideCheckerEnableLane2		1	
	0	HostSideCheckerEnableLane1		1	
164	7-4	HostSideCheckerPatternSelectLane2	The Pattern IDs are summarized below: 0: PRBS-31Q 1: PRBS-31 2: PRBS-23Q 3: PRBS-23 4: PRBS-15Q 5: PRBS-15 6: PRBS-13Q	0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane1		0x0	
165	7-4	HostSideCheckerPatternSelectLane4		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane3		0x0	

166	7-4	HostSideCheckerPatternSelectLane6	7: PRBS-13 8: PRBS-9Q 9: PRBS-9 10: PRBS-7Q 11: PRBS-7 12: SSPRQ 13: Reserved 14: Custom 15: User Pattern	0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane5		0x0	
167	7-4	HostSideCheckerPatternSelectLane8		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane7		0x0	
178	3-2	HostPRBSCheckerClockSource	0: Recovered clocks from Respective Host Lane/Datapaths are used 1: All lanes use Internal Clock 2: All lanes use reference clock 3: reserved	0b00	RO (VR)

4.5.1 PRBS Checker Lock Status

In PRBS Checker mode, the loss of lock (LOL) status is reported in register 138 of Page 14h.

Address	Bit	Name	Description	Default Value	Type
138	7	PatternCheckerLOLFlagHostLane8	-0b: no LOL is detected (Locked) -1b: LOL is detected (not Locked)	0	RO
	6	PatternCheckerLOLFlagHostLane7		0	
	5	PatternCheckerLOLFlagHostLane6		0	
	4	PatternCheckerLOLFlagHostLane5		0	
	3	PatternCheckerLOLFlagHostLane4		0	
	2	PatternCheckerLOLFlagHostLane3		0	
	1	PatternCheckerLOLFlagHostLane2		0	
	0	PatternCheckerLOLFlagHostLane1		0	

4.6 Loopback

The Host side loopback control registers are described in the table below. These registers are present in Page 13h. The Loopback mode is the default mode of the module. Writing 0x00 to register 183 will enable the PRBS Generator mode.

Address	Bit	Name	Description	Default Value	Type
183	7	HostSideInputLoopbackEnableLane8	-0b: PRBS Generator / Checker mode -1b: Retimed Loopback Mode Writing 1 to any of the register 183 bits will enable the Loopback mode on all channels.	1	RW (VR)
	6	HostSideInputLoopbackEnableLane7		1	
	5	HostSideInputLoopbackEnableLane6		1	
	4	HostSideInputLoopbackEnableLane5		1	
	3	HostSideInputLoopbackEnableLane4		1	
	2	HostSideInputLoopbackEnableLane3		1	
	1	HostSideInputLoopbackEnableLane2		1	
	0	HostSideInputLoopbackEnableLane1		1	

4.7 CDB.

The module advertises CDB support and CDB commands and timing.
The CDB support firmware upgrade through EPL writes.
The commands that are supported:

- CMD 0100h: Get Firmware Info
- CMD 0101h: Start Firmware Download
- CMD 0102h: Abort Firmware Download
- CMD 0104h: Write Firmware Block EPL
- CMD 0107h: Complete Firmware Download
- CMD 0109h: Run Firmware Image
- CMD 010Ah: Commit Firmware Image

4.8 BER/SNR

The BER and SNR data and control are described in this section.

4.8.1 Error Information Reset and Update Period

The error information reset and update period control register 177 is present in Page 13h.

Address	Bit	Name	Description	Default Value	Type
177	5	ResetErrorInformation	This bit is used to clear the error counters and restart accumulation of errors. -13h:177.5 = 1b: Currently accumulating error statistics identified by DiagnosticsSelector 01h to 05h are frozen -13h:177.5 = 0b: Error statistics identified by Selectors 01h-05h are reset to 0 When configuration in 13h:129.3=0b there is only 1 timer for all lane and all banks. Setting this bit to 1b: single gate timer is stopped Setting this bit to 0b: starts the single gating timer	0	RW (VR)
	0	UpdatePeriodSelect	Time between incremental updates to intermediate error counting results during a longer gating period 0b: 1 sec update interval 1b: 5 sec update interval	1	RW (NVR)

4.8.2 Diagnostics Selector

The diagnostics selector is described in the table below. It is controlled from register 128 of Page 14h. This register controls the content of diagnostics data registers.

Address	Bit	Name	Description	Default Value	Type
128	7-0	DiagnosticsSelector	Select content of Diagnostics Data in bytes 192-255: -0x02: Host Lane 1-4 errors and total Bits counters (gives the host the ability to read the running BER while gating is in progress) -0x03: Host Lane 5-8 errors and total Bits counters (gives the host the ability to read the running BER while gating is in progress) -0x06: Host/Media Input Lane 1-8 SNR	0	RW (VR)

4.8.3 BER Diagnostics

The tables below show the registers reporting the errors count and the total bit counters for each channel. The mentioned registers are present in Page 14h. The reported channels are related to the value set in register 128 of page 14h as detailed in section 4.8.2.

For detailed info on how error count is reported, refer to section 4.5.

In case of 14h:128 = 0x02, check the table below.

Address	size	Name	Description	Default Value	Type
192-199	8	HostSideErrorCountLane1	U64 Little-endian error count Lane 1	0	RO (VR)
200-207	8	HostTotalBitsCountLane1	U64 Little-endian total bit count 1	0	
208-215	8	HostSideErrorCountLane2	U64 Little-endian error count Lane 2	0	
216-223	8	HostTotalBitsCountLane2	U64 Little-endian total bit count 2	0	
224-231	8	HostSideErrorCountLane3	U64 Little-endian error count Lane 3	0	
232-239	8	HostTotalBitsCountLane3	U64 Little-endian total bit count 3	0	
240-247	8	HostSideErrorCountLane4	U64 Little-endian error count Lane 4	0	
248-255	8	HostTotalBitsCountLane4	U64 Little-endian total bit count 4	0	

In case of 14h:128 = 0x03, check the table below.

Address	size	Name	Description	Default Value	Type
192-199	8	HostSideErrorCountLane5	U64 Little-endian error count Lane 5	0	RO (VR)
200-207	8	HostTotalBitsCountLane5	U64 Little-endian total bit count 5	0	
208-215	8	HostSideErrorCountLane6	U64 Little-endian error count Lane 6	0	
216-223	8	HostTotalBitsCountLane6	U64 Little-endian total bit count 6	0	
224-231	8	HostSideErrorCountLane7	U64 Little-endian error count Lane 7	0	
232-239	8	HostTotalBitsCountLane7	U64 Little-endian total bit count 7	0	
240-247	8	HostSideErrorCountLane8	U64 Little-endian error count Lane 8	0	
248-255	8	HostTotalBitsCountLane8	U64 Little-endian total bit count 8	0	

4.8.4 SNR diagnostics

The table below shows the registers reporting the SNR for each channel at the host side. The mentioned registers are present in Page 14h. In this case 14h:128 should be set to 0x06, as described in section 4.8.2.

Address	size	Name	Description	Default Value	Type
208-209	2	HostSideSNRLane1	U16 Little-endian in units of 1/256dB host lane 1 real time SNR	0	RO (VR)
210-211	2	HostSideSNRLane2	U16 Little-endian in units of 1/256dB host lane 2 real time SNR	0	
212-213	2	HostSideSNRLane3	U16 Little-endian in units of 1/256dB host lane 3 real time SNR	0	
214-215	2	HostSideSNRLane4	U16 Little-endian in units of 1/256dB host lane 4 real time SNR	0	
216-217	2	HostSideSNRLane5	U16 Little-endian in units of 1/256dB host lane 5 real time SNR	0	
218-219	2	HostSideSNRLane6	U16 Little-endian in units of 1/256dB host lane 6 real time SNR	0	
220-221	2	HostSideSNRLane7	U16 Little-endian in units of 1/256dB host lane 7 real time SNR	0	
222-223	2	HostSideSNRLane8	U16 Little-endian in units of 1/256dB host lane 8 real time SNR	0	

4.9 TX and RX Control Fields

This section lists the specific controls for each TX and RX lane. The control registers mentioned in this section are present in Page 10h.

Address	Bit	Name	Description	Default Value	Type
129	7	InputPolarityFlipTx8	Input Polarity Flip control: -0b: No TX input polarity flip -1b: Tx input polarity flip	0	RW (VR)
	6	InputPolarityFlipTx7		0	
	5	InputPolarityFlipTx6		0	
	4	InputPolarityFlipTx5		0	
	3	InputPolarityFlipTx4		0	
	2	InputPolarityFlipTx3		0	
	1	InputPolarityFlipTx2		0	
	0	InputPolarityFlipTx1		0	
137	7	OutputPolarityFlipRx8	Output Polarity Flip control: -0b: No RX Output polarity flip -1b: RX Output polarity flip	0	RW (VR)
	6	OutputPolarityFlipRx7		0	
	5	OutputPolarityFlipRx6		0	
	4	OutputPolarityFlipRx5		0	
	3	OutputPolarityFlipRx4		0	
	2	OutputPolarityFlipRx3		0	
	1	OutputPolarityFlipRx2		0	
	0	OutputPolarityFlipRx1		0	
138	7	OutputDisableRx8	Output Disable control: -0b: RX Output enabled -1b: RX Output disabled	0	RW (VR)
	6	OutputDisableRx7		0	
	5	OutputDisableRx6		0	
	4	OutputDisableRx5		0	
	3	OutputDisableRx4		0	
	2	OutputDisableRx3		0	
	1	OutputDisableRx2		0	
	0	OutputDisableRx1		0	

4.10 Advanced Configuration

The high-speed interface configuration such as taps, gray mapping, signal type and baud rate can be controlled from Page B8h. After any parameter is changed, apply configuration should be performed for the new settings to take effect which can be done by putting the module in low power mode then back to high power mode.

Address	bit	Name	Description	Default Value	Type
128 (Page B8h)	2	Taps control	0: 3-Taps FIR Mode 1: 6-Taps FIR Mode	1	RW (NVR)
	1	Gray mapping	0: Gray mapping disabled 1: Gray mapping enabled	1	
	0	Signal type	0: PAM4 signal type 1: NRZ signal type	0	
129 (Page B8h)	7-0	Baud Rate Select	0: 25.78125 GBaud 1: 26.5625 GBaud 2: 53.125 GBaud 3: 56.25 GBaud 4: 106.25 GBaud	0x04	
131 (Page B8h)	0	Configuration mode	0: CMIS controls the high-speed interface thorugh DataPath state machine, and controls the RXOUT EQ 1: User EEPROM pages B0 to B8 controls the above	0	

Note: DSP configuration and RXOUT equalization are by default controlled from the CMIS registers in **Page 10h**.

If the user wants to use the advanced configuration, register 131 of **Page B8h** must be set to 1. This is an NVM register and only needs to be set once for switching between CMIS and advanced mode. To apply configuration, put the module in low power mode then high power mode.

4.10.1 Precoder and Extended Reach

Precoder control and Extended Reach (ER) enable/disable can be done using register 130 of Page B8h:

Address	Bit	Name	Description	Default Value	Type
130 (Page B8h)	7-0	Precoder and ER enable/disable	Write **0x01**: Enable Precoder and ER (disable NR). Write any other value: Disable Precoder and ER (enable NR)	0x00	RW (NVR)

In case Precoder and ER are not enabled from register 130 (Register 130 has a value other than 0x01), and if Register 131 (Page B8h) = 0x01, it is possible to control ER and Precoder from Register 128 (Page B8h) bits 3 and 4:

Address	Bit	Name	Description	Default Value	Type
128 (Page B8h)	4	ER/NR control	0: Disable ER (enable NR) 1: Enable ER (disable NR) (Works if Page B8h Register 130 ≠ 0x01 and Register 131 = 0x01)	0	RW (NVR)

	3	Precoder control	0: Disable precoder 1: Enable precoder (Works if Page B8h Register 130 ≠ 0x01 and Register 131 = 0x01)	0	

4.10.2 Link Training

Link Training (LT) is supported in the ML4064-AL7I/R-224, and can be enabled or disabled using Register 180 of Page 03.
The Link Training setting is stored in non-volatile memory (Register 180, Page 03), therefore the selected configuration is retained after reset or power cycle.
At DataPath initialization, LT is enabled or disabled according to the value stored in the register.

Address	Bit	Name	Description	Default Value	Type
180 (Page 03)	7-0	LT enable/disable	Write **0x01**: Enable LT. Write **0x00**: Disable LT.	0x00	RW (NVR)

Note: When Link Training is enabled, DSP power consumption may increase. If the total requested power exceeds the supported module limit (~43W), the firmware automatically limits the applied power to remain within the allowed range. This may include modifying the programmed values in the power control registers.

4.11 Advanced Channel Configuration

RX output channels can be configured separately to tune the RX output signals.
Each channel is controlled from a separate page, from B0h to B7h, for the register address range from 128 to 139.

The table below shows the page number corresponding to each channel.

Page Address	Description
B0	RXOUT 1 control page
B1	RXOUT 2 control page
B2	RXOUT 3 control page
B3	RXOUT 4 control page
B4	RXOUT 5 control page
B5	RXOUT 6 control page
B6	RXOUT 7 control page
B7	RXOUT 8 control page

After the page is the set, the corresponding parameters can be controlled, as described in the table below.
Any change of the value in one of the following registers needs to apply configuration by putting the module in low power mode then back to high power mode.

The table below corresponds to Page B0h (RXOUT 1 control page).

Address	size	Name	Description	Default Value	Type
128	1	Pre3 (MSB)	16-bit signed value	0x00	RW (NVR)
129	1	Pre3 (LSB)		0x00	
130	1	Pre2 (MSB)	16-bit signed value	0x00	
131	1	Pre2 (LSB)		0x00	
132	1	Pre1 (MSB)	16-bit signed value	0xFF	
133	1	Pre1 (LSB)		0xDC	
134	1	Main (MSB)	16-bit signed value	0x00	
135	1	Main (LSB)		0x84	
136	1	Post1 (MSB)	16-bit signed value	0x00	
137	1	Post1 (LSB)		0x00	
138	1	Post2 (MSB)	16-bit signed value	0x00	
139	1	Post2 (LSB)		0x00	

Note:

- Main tap is expected to be positive and Pre1 and Post1 taps are expected to be negative.
- Main tap is expected to be greater than all other taps.
- Pre3 tap is expected to be within [-12,0].
- NRZ mode absolute sum limit is 127 and PAM4 mode absolute sum limit is 168.

5 OSFP Pin Allocation

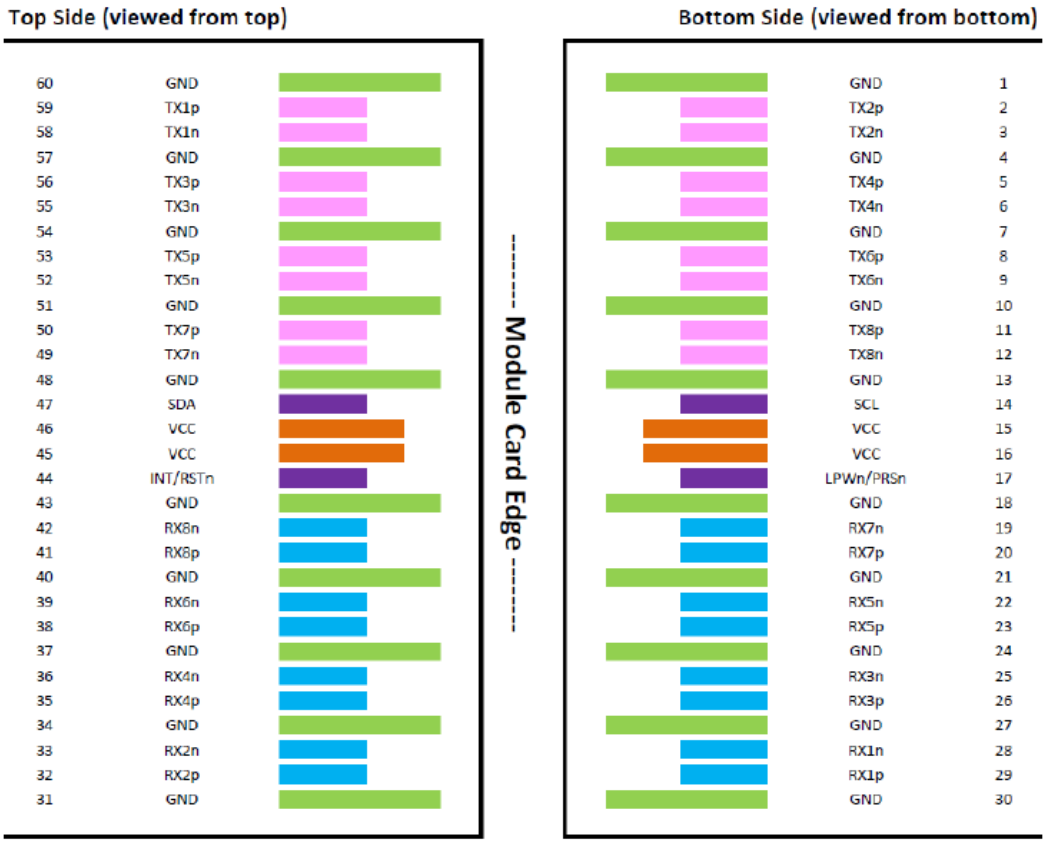


Figure 14: OSFP Module Pad Layout

6 Mechanical Dimensions

6.1 ML4064-AL7I-224

The ML4064-AL7I-224 comes in a type 2 OSFP1600 IHS shell.

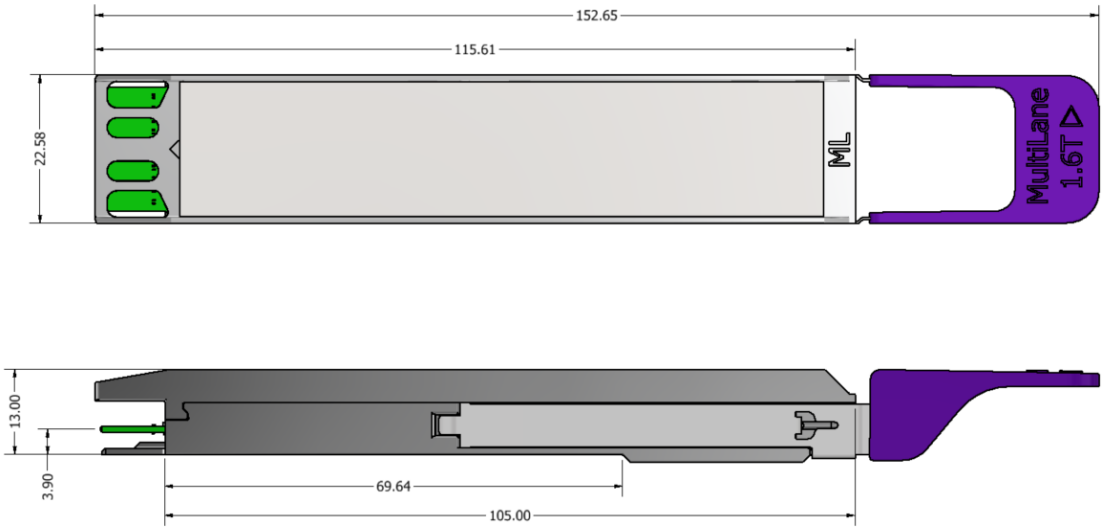


Figure 15: ML4064-AL7I-224 Mechanical Dimensions

6.2 ML4067-AL7R224

The ML4064-AL7R-224 comes in a type 2 OSFP1600 RHS shell.

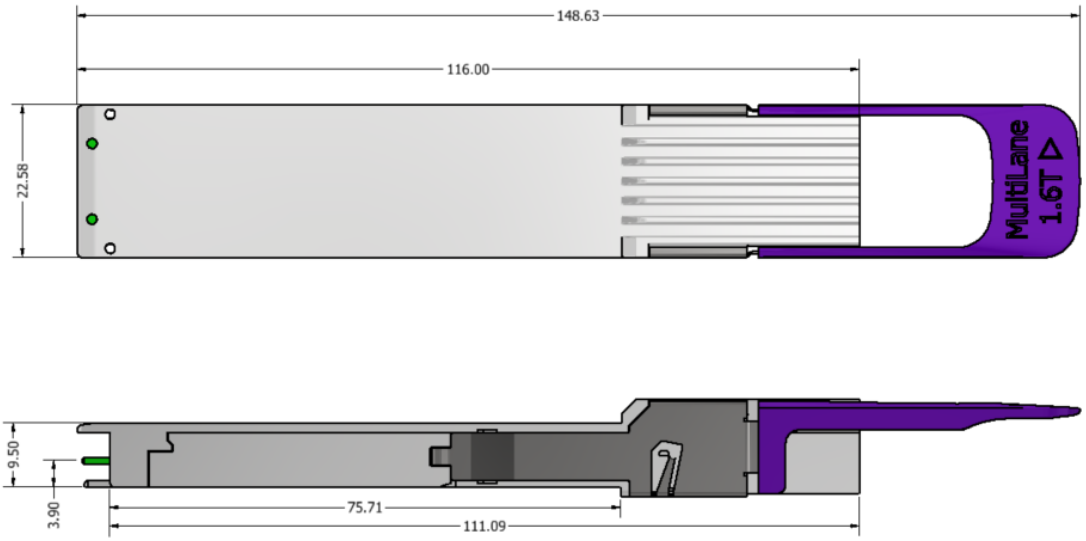


Figure 16: ML4064-AL7R-224 Mechanical Dimensions

7 FW Revision

- For HW RevA1:

FW Release	Upgrades
V1.0	• Initial FW release
V1.1	• Changed content of Register 201 Page 00
V1.2	• Updated low-temp alarm and warning threshold value • Support LOS, CDR LOL flags • Support SNR reading

- For HW RevB1:

FW Release	Upgrades
V1.0	• Initial FW Release • Vendor Revision is *2 0* • Available power modes: Modes 1, 2 & 3
V1.1	• Added support of power Mode 4

8 HW Revision

HW Version	Changes
A1	• Initial hardware version
B1	• Added paddle card power spots • Using DSP package B

Revision History

Revision Number	Date	Description
1.0	4/1/2026	• Initial version • This version reflects the changes for RevB